VV5411 & VV6411

Mono and Colour Digital Video CMOS Image Sensors

The VV5411/VV6411 are multi-format digital output imaging devices based on STMicroelectronics's unique CMOS sensor technology. Both sensors require minimal support circuitry. The VV6411 and VV5411 are replacements for the VV6410 and VV5410, and are intended to enable even more cost-effective imaging solutions. The 6411 also uses more modern colour filter material to ensure optimum colour performance

VV5411 (monochrome) and VV6411 (colourised) produce digital video output. The video streams from both devices contain embedded control data that can be used to enable frame grabbing applications as well as providing input data for an external exposure controller.

VV6411 can interface to a range of STMicroelectronics co-processors. A USB camera can be realised by partnering VV6411 with TV0676. A low cost digital stills camera can be produced by operating VV6411 with STV0680B-003. Please contact STMicroelectronics for ordering information on all of these products.

Both VV5411 and VV6411 are initialised in a power saving mode and must be enabled via the I^2C interface before they can produce a video output. The I^2C interface allows the master coprocessor to reconfigure the device and control exposure and gain settings.

USB systems are catered for with an ultra low power, pin driven, suspend mode.

The on board regulator can supply sufficient current drive to power external components, (e.g. the video coprocessor).

Applications

- PC camera
- Personal digital assistant
- Digital stills cameras

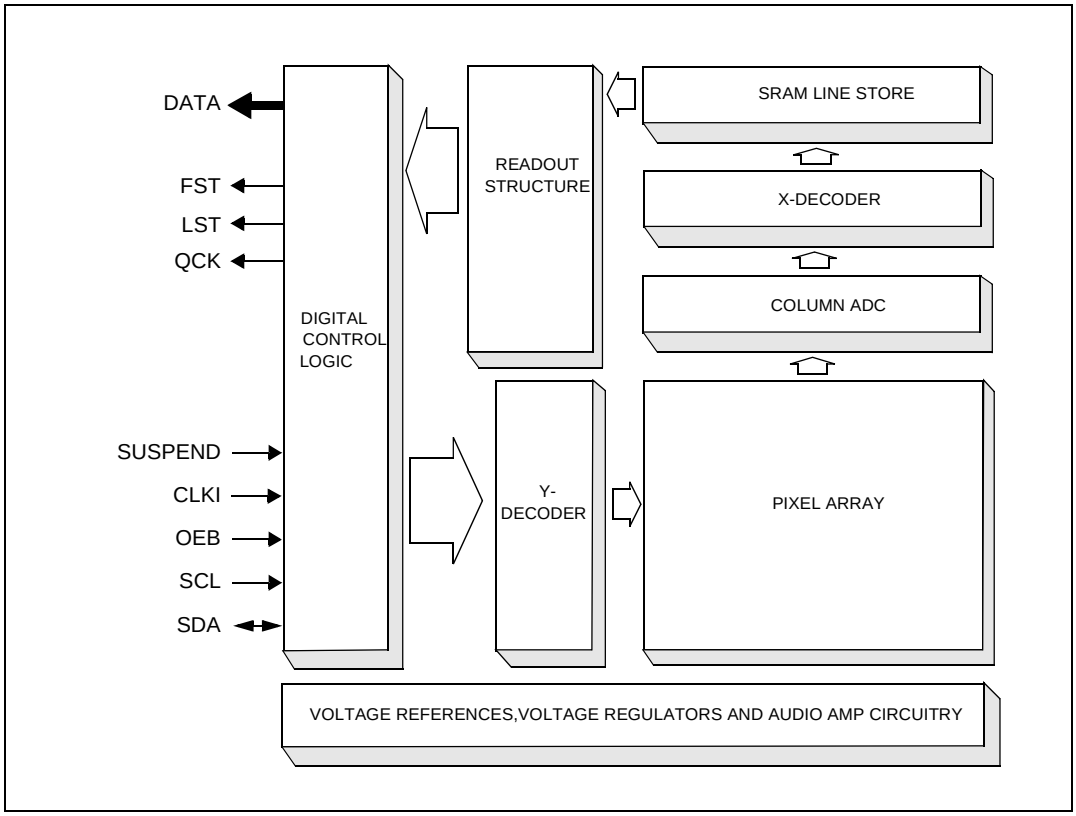
Key Features

- 3.3V operation
- Multiple video formats available
- Pan tilt/sub sampled image features
- On board 10 bit ADC
- On board voltage regulator
- Low power suspend mode for USB systems
- Automatic black and dark calibration
- On board audio amplifier
- I^2C communications

Specifications

Effective image sizes after colour processing	352 x 288 (CIF,PAL) 176 x 144 (QCIF)
Pixel resolution	up to 356 x 292
Pixel size	7.5µm x 6.9µm
Array size	2.73mm x 2.04mm
Exposure control	+81dB
Analogue gain	+12dB (recommended max)
SNR	c.56dB
Random Noise	1.7mV
Sensitivity (Green channel)	2.75V/lux.sec
Dark Signal	67mV/sec
VFPN	0.53mV
Supply voltage	3.0V- 6.0V DC +/– 10%
Supply current	<40mA (max,CIF@30fps) <100µA (suspend mode)
Operating temperature (ambient)	0^oC - 40^oC
Package type	36pin CLCC

Functional block diagram



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Document Revision History

Table 1: Document Revision History

Revision	Date	Comments
3.0	26/03/2001	Original release (datasheet derived from Version 3.0 of the 410 datasheet)
A	04/05/01	Copy of Revision 3 of the datasheet Also incorporate typo/formatting corrections Pin out/bonding numbering for 44pin package corrected Defect specification updated to reflect new test program Voltage regulator description corrected
A version	27/05/02	Whole document reformatted with ST actual corporate template Addition of: *Figure 57: 36 pin CLCC package drawing on page 109* Correction of figures for design reference: *Chapter 15: Recommended VV5411/6411 support circuits on page 110* Removed all references to OTQFP44 package. *Chapter 7: Digital Video Interface Format on page 31* Detailed the timing in 8-bit data mode *Chapter 12: Defect Categorization on page 100* Modified test acceptance of minor/major couplets in inner and outer piel areas.

1 Introduction

1.1 Overview

VV5411/VV6411 is a CIF format CMOS image sensor. The VV5411 sensor is the basic monochrome device and VV6411 is the colorized variant. The operations of VV5411 and VV6411 are very similar but any difference is identified and explained.

VV6411 can output digital colorized pixel data at frame and line rates compatible with either NTSC or PAL video standards. VV5411 and VV6411 contain the same basic video timing modes. *Table 2* lists these video modes.

The various operating modes are detailed in *Chapter 2 in page 11*.

Important: VV5411 and VV6411's output video data stream only contains raw data. Further video formatting is required to generate an analogue video PAL or NTSC signal. For the VV6411, additional color processing is also required to produce a usable color image.

Table 2: Video modes

Mode	Input Clock (MHz)[a]	System Clock Divisor	Image Size	Line Time (µs)	Lines per Frame	Frame Rate (fps)
QCIF - 25 fps	8.00	8	180 x 148	250.00	160	25.00000
QCIF - 30 fps	8.00	8	180 x 148	208.00	160	30.04807
QCIF - 60 fps	16.00	8	180 x 148	104.00	160	60.09614
CIF - 25 fps	16.00	4	356 x 292	125.00	320	25.00000
CIF - 30 fps	16.00	4	356 x 292	104.00	320	30.04807
NTSC (3.2 fsc)	28.636360 / 2.5	2	306 x 244	63.555564	525	29.97003
PAL (3.2 fsc)	35.46895 / 2.5	2	356 x 292	63.999639	625	25.00014

a. The user can also provide a 24 MHz clock, rather than a 16 MHz clock, for the QCIF-60fps, CIF-25fps and CIF-30fps modes, which the sensor then internally divides by 1.5, (see data_format[22]), to give an effective input clock frequency of 16 MHz.

1.2 Exposure control

VV5411/VV6411 does not include any form of automatic exposure or gain control. To produce a correctly exposed image an exposure control algorithm must be implemented externally. New exposure values are written to the sensor via the I2C.

1.3 Digital Interface

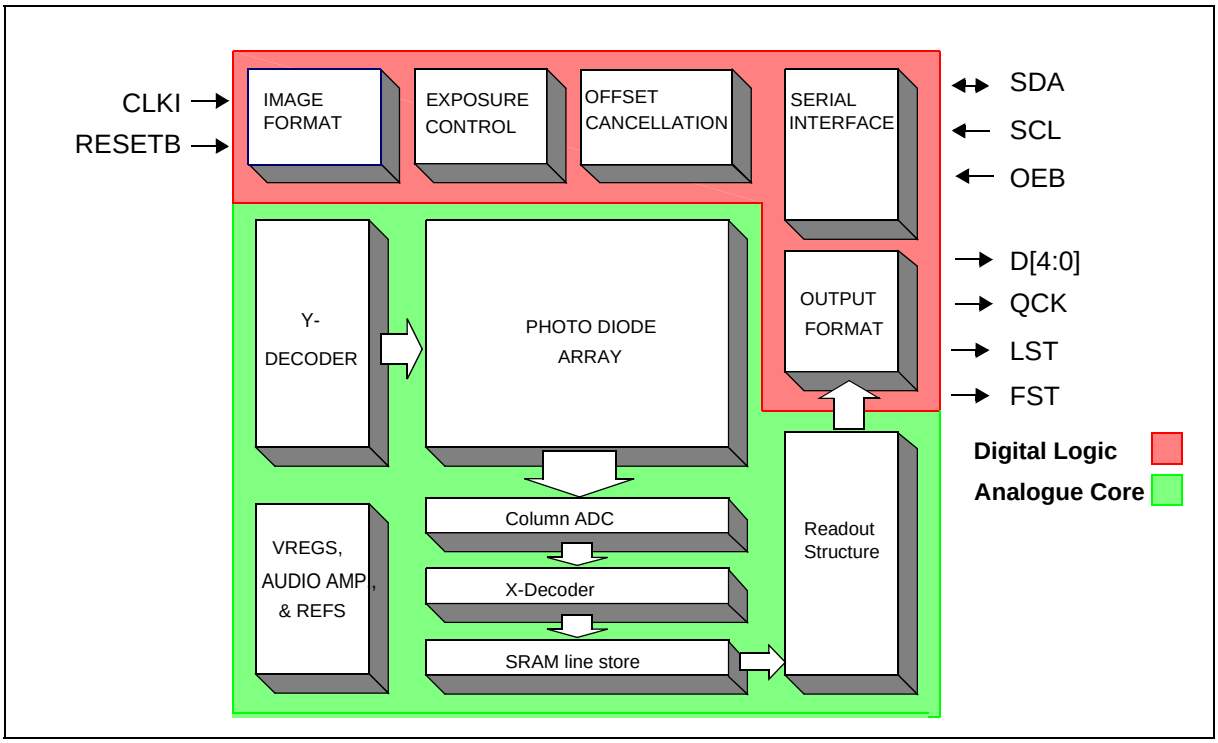
The sensor offers a flexible digital interface, with the following main components:

- a tri-stateable 5-wire data bus (D[4:0]) to send both video data and embedded timing references,
- 4-wire and 8-wire data bus alternatives. If the 8-wire option is selected, the FST/LST pins are reconfigured to output data information.

- A data qualification clock, QCK, which can be programmable via the I^2C to behave in different ways (Tri-stateable),
- A line start signal, LST (Tri-stateable),
- A frame start signal, FST (Tri-stateable),
- OEB tri-states all 5 data bus lines, D[4:0], the qualification clock, QCK, LST, FST and D[7].

A 2-wire I^2C (SDA,SCL) interface to control and set-up the device.

Figure 1: Block diagram of VV5411/VV6411 image sensor (5-wire output)



1.3.1 Digital data bus

Along with the pixel data, codes representing the start and end of fields and the start and end of lines are embedded within the video data stream to synchronize the processing system with the video data that the camera module is generating. *Chapter 7 in page 31* defines the format for the output video data stream.

1.3.2 Frame grabber control signals

To complement the embedded control sequences, the following independent set-ups for the data qualification clock (QCK), the line start signal (LST) and the field start signal (FST) signals are available:

- disabled,
- free-running,
- Qualify only the control sequences and the pixel data.
- Qualify the pixel data only.

There is also the choice of two different QCK frequencies where one is twice the frequency of the other.

- Fast QCK: the falling edge of the clock qualifies every 8, 5 or 4 bit blocks of data that make up a pixel value.

- Slow QCK: the rising edge qualifies 1st, 3rd, 5th, etc. blocks of data that make up a pixel value while the falling edge qualifies the 2nd, 4th, 6th etc. blocks of data. For example in 4-wire mode the rising edge of the clock qualifies the most significant nibbles while the falling edge of the clock qualifies the least significant nibbles.

1.3.3 I²C interface

The I²C provides complete control over sensor setup and operation.

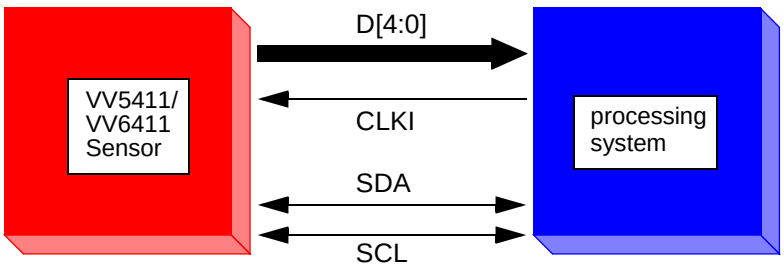
Chapter 8 in page 63 defines the I²C communications protocol and the register map of all the locations which can be accessed via the I²C.

1.4 Sensor/processing system interface options

There are 3 main ways of interfacing to the VV5411/VV6411 as illustrated below. Note that the described processing system could comprise other STMicroelectronics products such as microcontrollers or dedicated DSP devices.

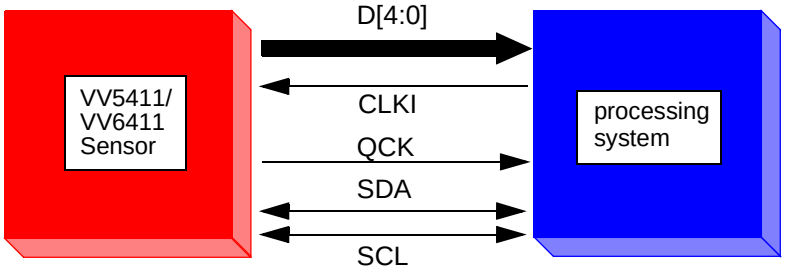
- The color processing system supplies the sensor clock, CLKI, and uses the embedded control sequences to synchronize with the frame and line level timings. Thus the host and sensor run-off derivatives of the same fundamental clock. During its power-up sequence, the sensor outputs a 101010... sequence on each of its data bus lines for the host to lock on to. This allows the processing system to determine the best sampling position of the video data.

1.



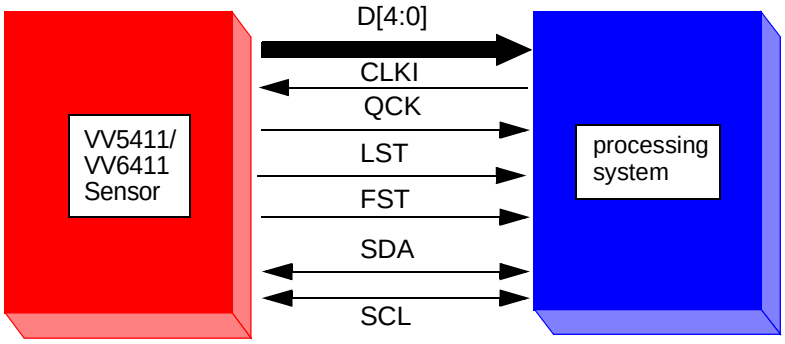
- The color processing system supplies the sensor clock, CLKI, and uses a free-running QCK supplied by the sensor to sample the incoming video data stream. The embedded control sequences are used to synchronize the frame and line level timings.

2.



- The color processing system supplies the sensor clock, CLKI, and uses FST, LST and the data only mode for QCK to synchronize with the incoming video data. This is primarily intended to interface with frame grabbers.

3.



1.5 Other features

1.5.1 Audio amplifier

AIN and AOUTP & AOUTN pins are the input and outputs for an audio amplifier, respectively.

1.5.2 Voltage regulator

The on-chip voltage regulator requires only a few external components to form a fully functional voltage regulator to 3.3V.

1.5.3 I^2C programmable pins

The FST and QCK pins can be reconfigured for the 2-bit state of a serial register. Then, the user can use these control bits to control a peripheral device, a motor or shutter mechanism for example.

2 Operating Modes

2.1 Video timing

The video format mode on power-up is CIF 30fps by default. After power-up, the mode can be changed by an I^2C command, with a write to the *video_timing* register. The frame/field rate is also programmable via the I^2C. Bit [3] of serial register [16] selects between 30 and 25 frames per second for the CIF modes and 60/50 fields per second for the digital and analog timing modes. Please note that the sensor can exit low power in ANY of the available video modes.

The number of video lines in each frame is the same (320) for all CIF modes. The slower frame rate (25 fps) is implemented by simply extending the line period from 416 pixel periods to 500 pixel periods.

Table 3 details the setup for each of the video timing modes. A serial write tothe serial register [16] forces the contents of other registers in the I^2C interface to change to the appropriate values, regardless of their present state. If for example, the required data output mode is different than the default for a particular video mode, a write to the appropriate register after the mode has changed restores the desired value.

Table 3: Video timing modes

Video mode	Clock (MHz)	System clock divisor	Video data	Line length	Field length	Data output mode
PAL (3.2 fsc)	28.636360 / 2.5	2	356 x 292	454	312/313	5-wire
NTSC (3.2 fsc)	35.46895 / 2.5	2	306 x 244	364	262/263	5-wire
CIF - 25 fps	16.0	4	356 x 292	500	320	5-wire
CIF - 30 fps	16.0	4	356 x 292	416	320	5-wire
QCIF - 25 fps	8.0	8	180 x 148	250	160	5-wire
QCIF - 30 fps	8.0	8	180 x 148	208	160	5-wire
QCIF - 60 fps	16.0	8	180 x 148	208	160	5-wire

2.1.1 Arbitration registers

When changing the operating video mode, a number of serial registers are forced into new states. See the complete list in *Table 4*.

Table 4: Arbitration registers

Arbitrated feature	Video mode selected/value automatically programmed							
	PAL	NTSC	CIF 25fps	CIF 30fps	PTQCIF 25fps	PTQCIF 30fps	SSQCIF 25fps	SSQCIF 30fps
Line length	453	363	499	415	249	207	249	207
Field length	311	261	319	319	159	159	159	159
System clock division	2	2	4	4	8	8	8	8
Free running qck[a]	yes	yes	no	no	no	no	no	no
Extra black lines[b]	yes	yes	no	no	no	no	no	no

a. The free running qck, slow by default, is enabled by writing 8'h04 to serial register [20].

b. The contents of the extra black lines are enabled on to the data bus by setting bit [5] of serial register [17]. If bit [0] of serial register [24] is reset, indicating that the preferred coprocessor device is not the VP3 device, (an STMicroelectronics coprocessor), then the extra black lines are enabled by default regardless of the basic video mode selected.

The registers that control the image position within the pixel array and also the order in which the pixels are read out have not been included in the table as their values are subject to a secondary series of registers (see *Section 2.2* and *Section 2.3*).

2.1.2 Input clock frequencies

It is recommended to use a 16 MHz clock to generate CIF-25fps,CIF-30fps and QCIF-60fps and a 8 MHz clock to generate QCIF-25fps and QCIF-30fps, however the sensor can adapt to a range of other input frequencies and still generate the required frame rates. For example, a 24 MHz clock can be used to generate CIF-30fps. The sensor can automatically divide the incoming clock by 1.5 by setting bit [7] of serial register [22], so that the internal clock generator logic still receives a 16 MHz clock.

Note that the clock division register is an 8 bit value, although the user only programs the lower nibble. The upper nibble is reserved for the clock divisor setting when changing the primary video mode. The lower nibble can be programmed to reduce the effective frame rate within each video mode.

The system clock divisor column in *Table 5* assumes that the programmable pixel clock divisor is set to the default of 0, implementing a divide by 1 of the internal pixel clock. If for example, the user requires a 15 fps CIF resolution image, a wide range of options achieves the same result.

Table 5: System clock divisor options

clk in (MHz)	Divide by 3/2 enabled?	System clock divisor	Pixel clock divisor	pclk (MHz)	Field Rate
8	no	4	1	2	15
12	yes	4	1	2	15
16	no	4	2	2	15
24	yes	4	2	2	15

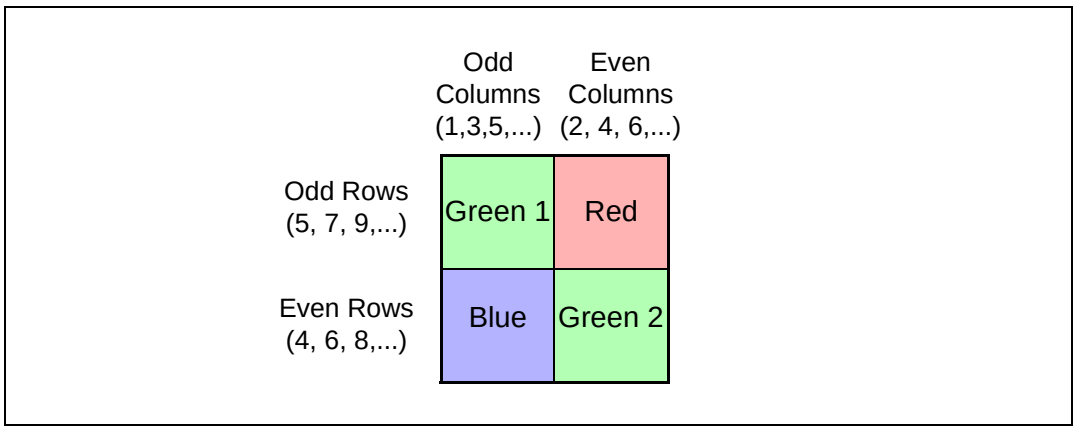
2.2 Pixel array

The physical pixel array is 364 x 296 pixels. The pixel size is 7.5 µm by 6.9 µm. The image size for NTSC is 306 x 244 pixels, for PAL and CIF it is 356 x 292 pixels, while for the QCIF modes the image size is 180 x 148 pixels. The remaining 4 physical columns on each side of the PAL image size prevent columns 1 and 2 in PAL/CIF modes from being distorted by the edge effects occuring when a pixel is close to the outer edge of the physical pixel array. Please note that these columns can be enabled as part of the visible image if the user operates the sensor in the pantilt QCIF mode.

Figure 3 shows how the 306 x 244 and 180 x 148 sub-arrays are aligned within the bigger 364 x 296 pixel array. The Bayer colorization pattern requires that the top-left corner of the pixel sub-array is always a Green 1 pixel. To preserve this Bayer color pattern, the NTSC sub-array has been offset relative to the centre of the array. The QCIF size images are centrally orientated.

Image read-out is very flexible. Section 2.3.2 - Section 2.3.5 describe the available options to the user. By default the sensor read out is configured to be horizontally ‘shuffled’ non-interlaced raster scan. The difference between the horizontally ‘shuffled’ raster scan order and the conventional raster is that the pixels of individual rows are re-ordered, with the odd pixels within a row read-out first, followed by the even pixels. This ‘shuffled’ read-out within a line groups pixels of the same color (according to the Bayer pattern - *Figure 2*) together, reducing cross talk between the color channels. This option is on by default and is controllable via the I^2C interface. The horizontal shuffle option is usually only selected with the color sensor variant, VV6411.

Figure 2: Bayer colorization pattern (VV6411 only)



2.3 X-offset and Y-offset

The image information is retrieved from the pixel array via a 2 dimensional address. The x and y address busses count from a starting point described by x-offset, y-offset up to a maximum count in x and y that is determined by the image size. The count order and the count step size depend on the special image format parameters as described below. The detailed control of the x and y address counters is entirely handled by the sensor logic.

The visible array size is 364 columns by 296 rows (see *Figure 3*). The PAL and CIF images are sized, 356 columns by 292 rows, thus we have a “border” of visible pixels that we do not read out if either of these modes are selected.

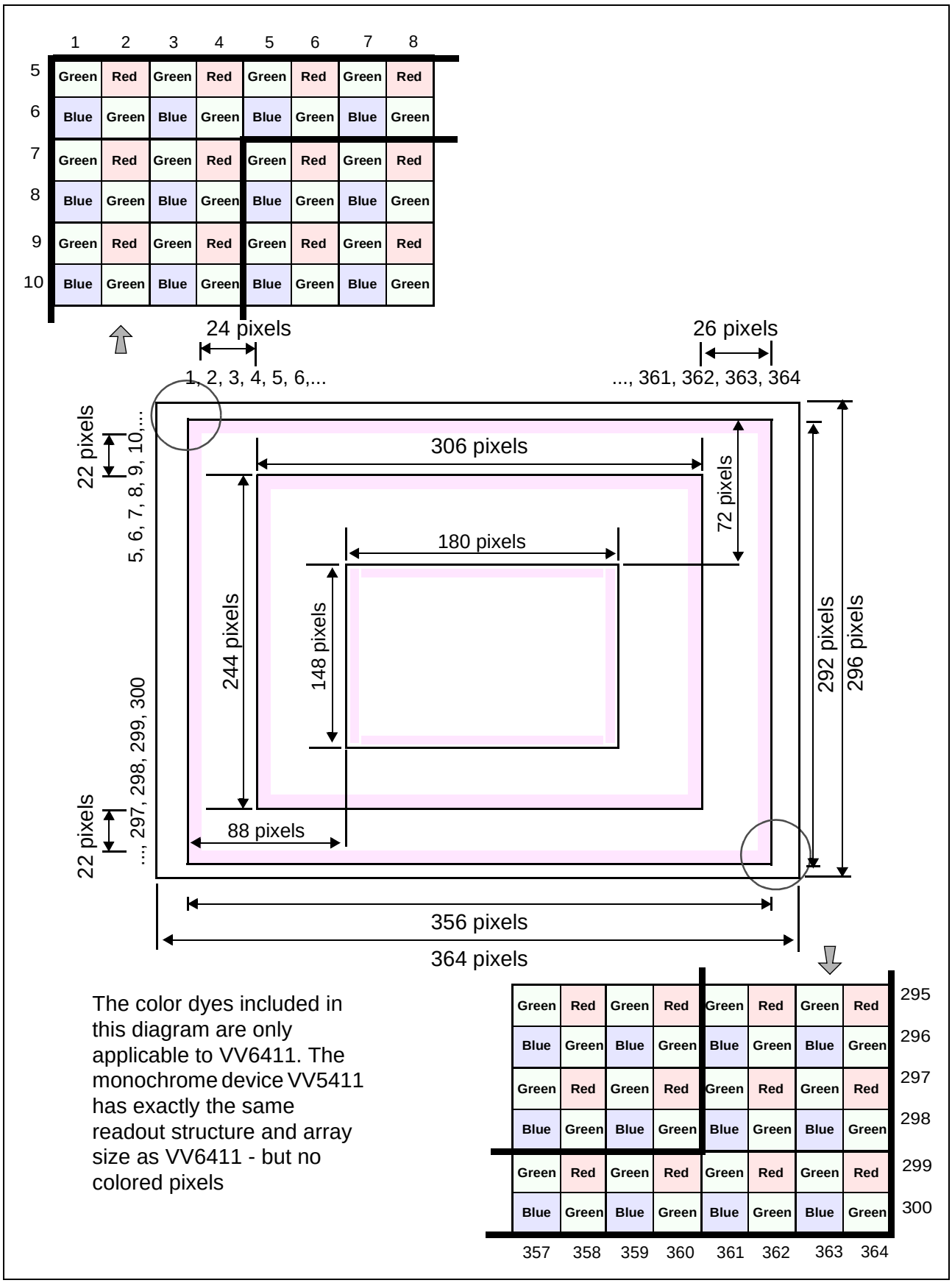
Images read out of the sensor are always “centred” on the array, therefore we allow a border of 4 columns at either end of the image in the x-direction and a border of 2 rows at the top and bottom of the image in the y-direction. The pantilt QCIF and NTSC video modes are similarly centred within the full size array.

For all the modes, except the pantilt QCIF mode, the x and y offset coordinates are fixed. If the user selects the pantilt QCIF mode then they may specify x and y-offsets in the range:

- 1 <= xoffset <= 185
- 5 <= yoffset <= 149

The sensor will automatically clip out values with the specified ranges. The y addresses inferior to 5 are reserved for the sensor black lines and the y address greater than 296 are reserved for the sensor dark lines. Neither the black lines nor the dark lines contain visible image data.

Figure 3: Image readout formats



2.3.1 Image readout parameters

The available parameters to process the sensor readout are the following:

- shuffle horizontal readout, enabled by setting bit [7] of serial register [17]
- mirror horizontal readout, enabled by setting bit [3] of serial register [22]
- shuffle vertical readout, enabled by setting [2] or serial register [22]
- flip vertical readout, enabled by setting [4] of serial register [22].

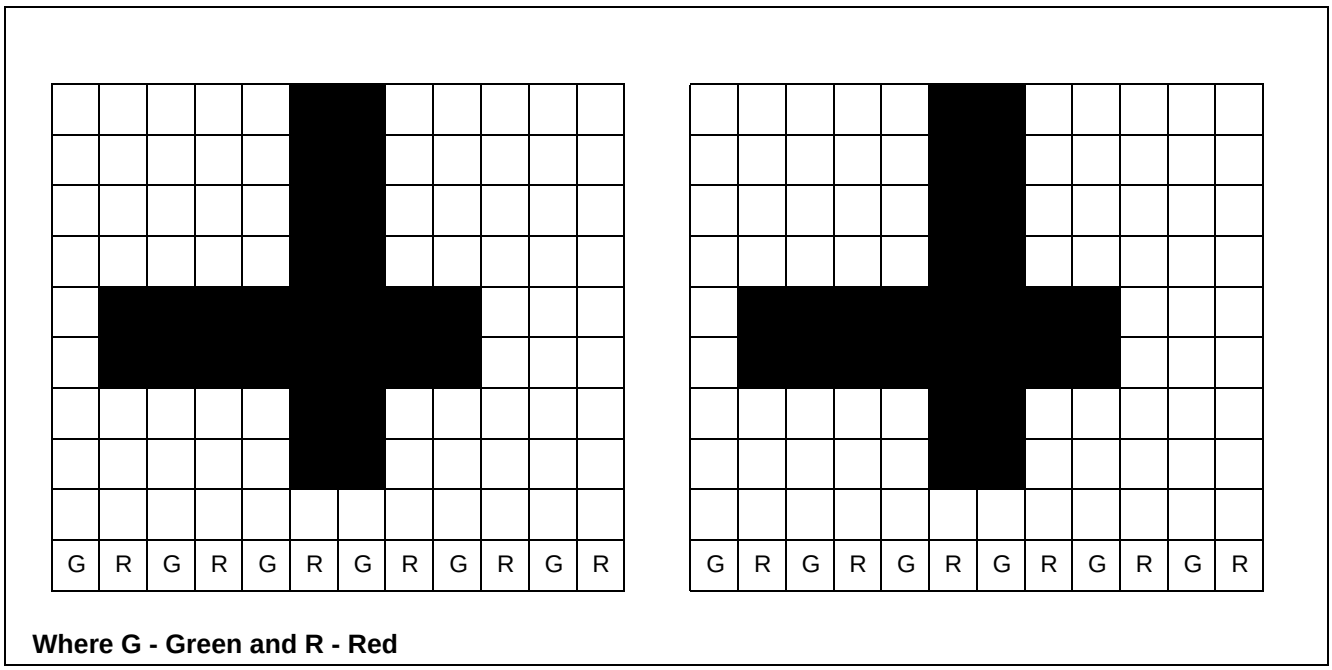
The effect of each of these parameters is probably best described via a series of diagrams, see Section 2.3.2 - Section 2.3.5 below.

Although these above features can be combined with one another, we describe the special image readout parameters one at a time.

2.3.2 Horizontal shuffle

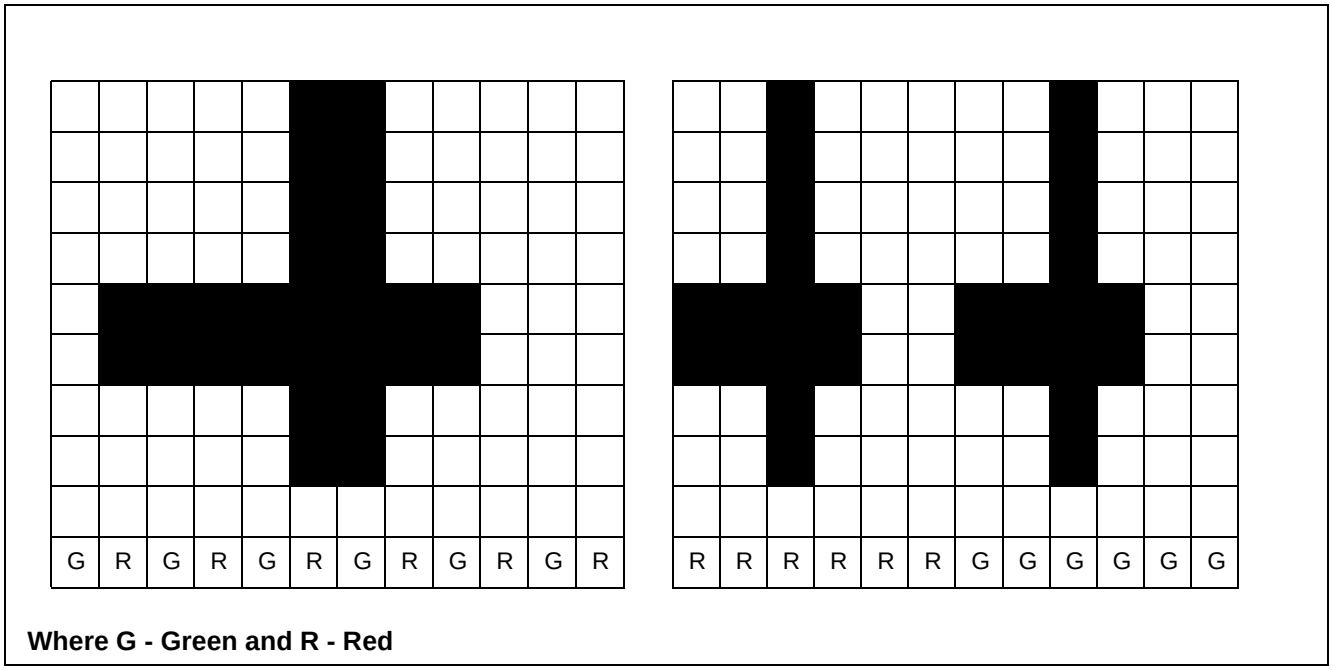
Figure 4 is the reference figure representing the image readout without any of the optional image parameters, shuffle or mirror, selected. *Figure 5* shows how the image is displayed when the horizontal shuffle bit has been selected. Note that the even columns (column 2,4,6 etc.) are read out first, followed by the odd columns (1,3,5,7 etc.).‘

Figure 4: Standard image read out



Where G - Green and R - Red

Figure 5: Horizontal shuffle enabled

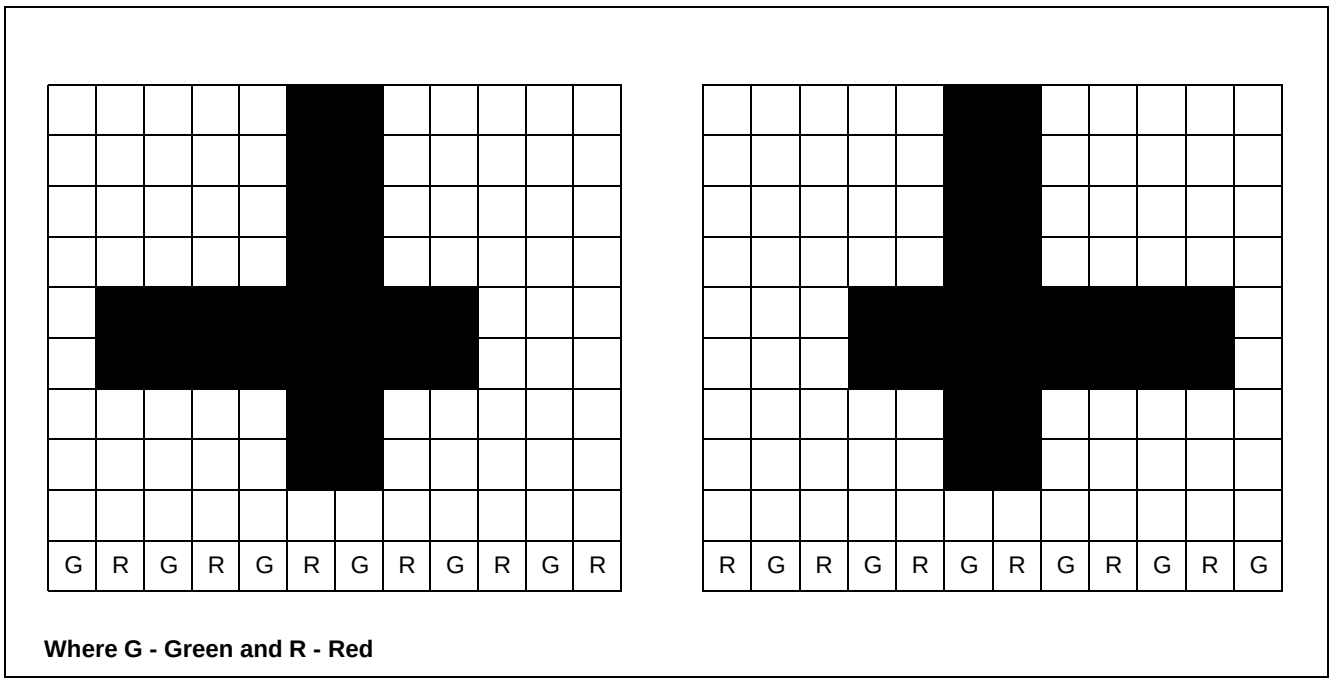


Where G - Green and R - Red

2.3.3 Horizontal mirror

Figure 6 shows the output image with the horizontal mirror feature enabled. Note that the columns are read out in reverse order.

Figure 6: Horizontal mirror enabled

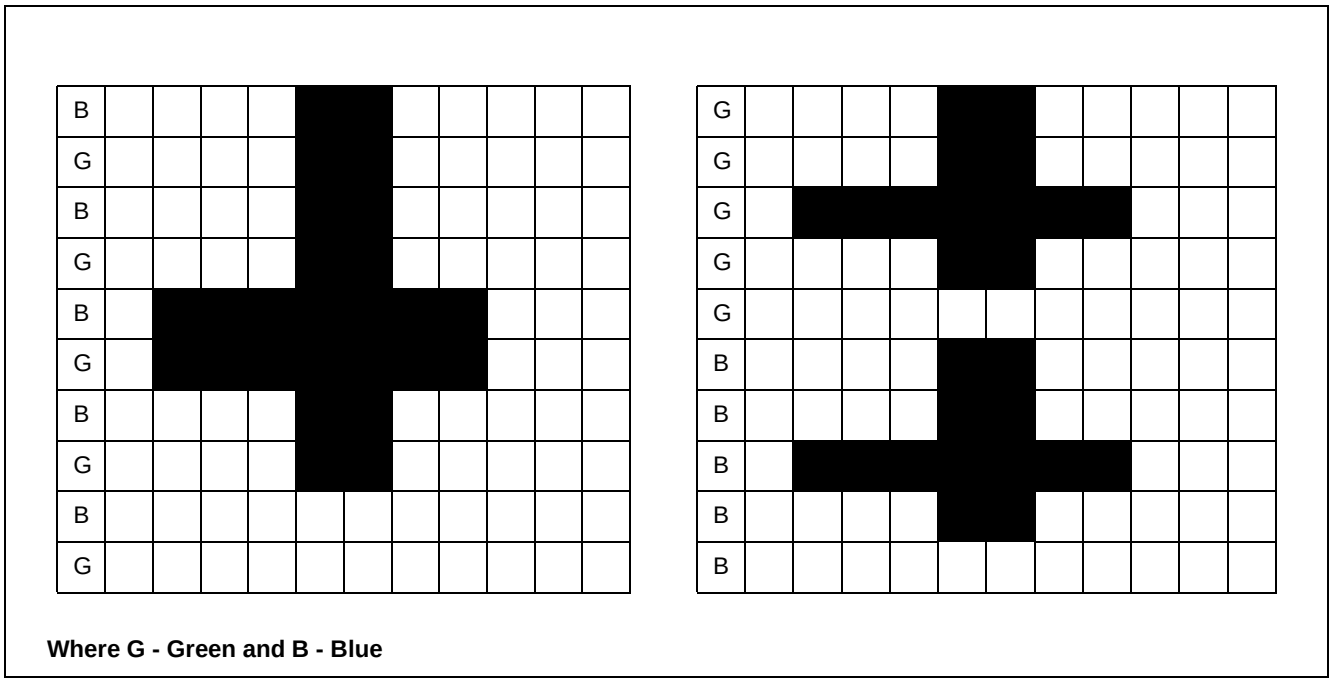


Where G - Green and R - Red

2.3.4 Vertical shuffle

Figure 7 shows the output image with the vertical flip feature enabled. Note that the even rows (rows 2,4,6 etc.) are read out first followed by the odd rows (rows 1,3,5 etc.

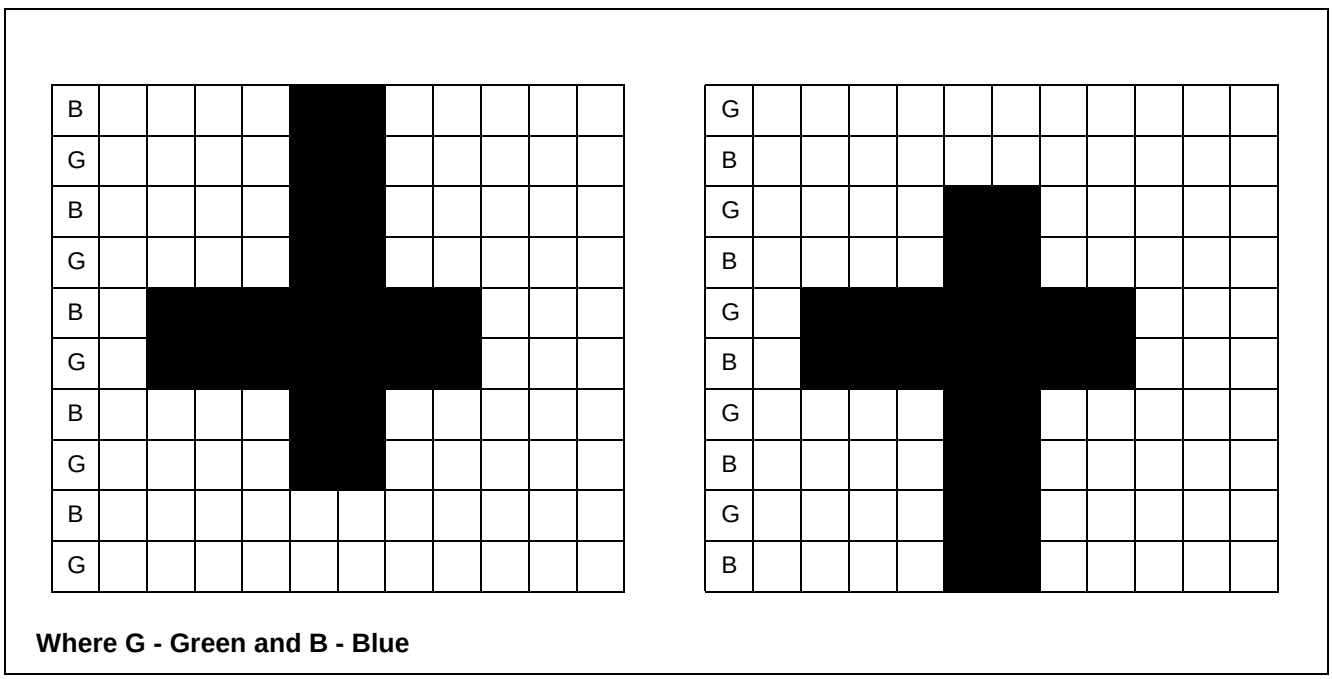
Figure 7: Vertical shuffle enabled



2.3.5 Vertical flip

Figure 8 shows the output image with the vertical flip feature enabled. Note that the rows are read out in reverse order.

Figure 8: Vertical flip enabled



2.4 QCIF output modes

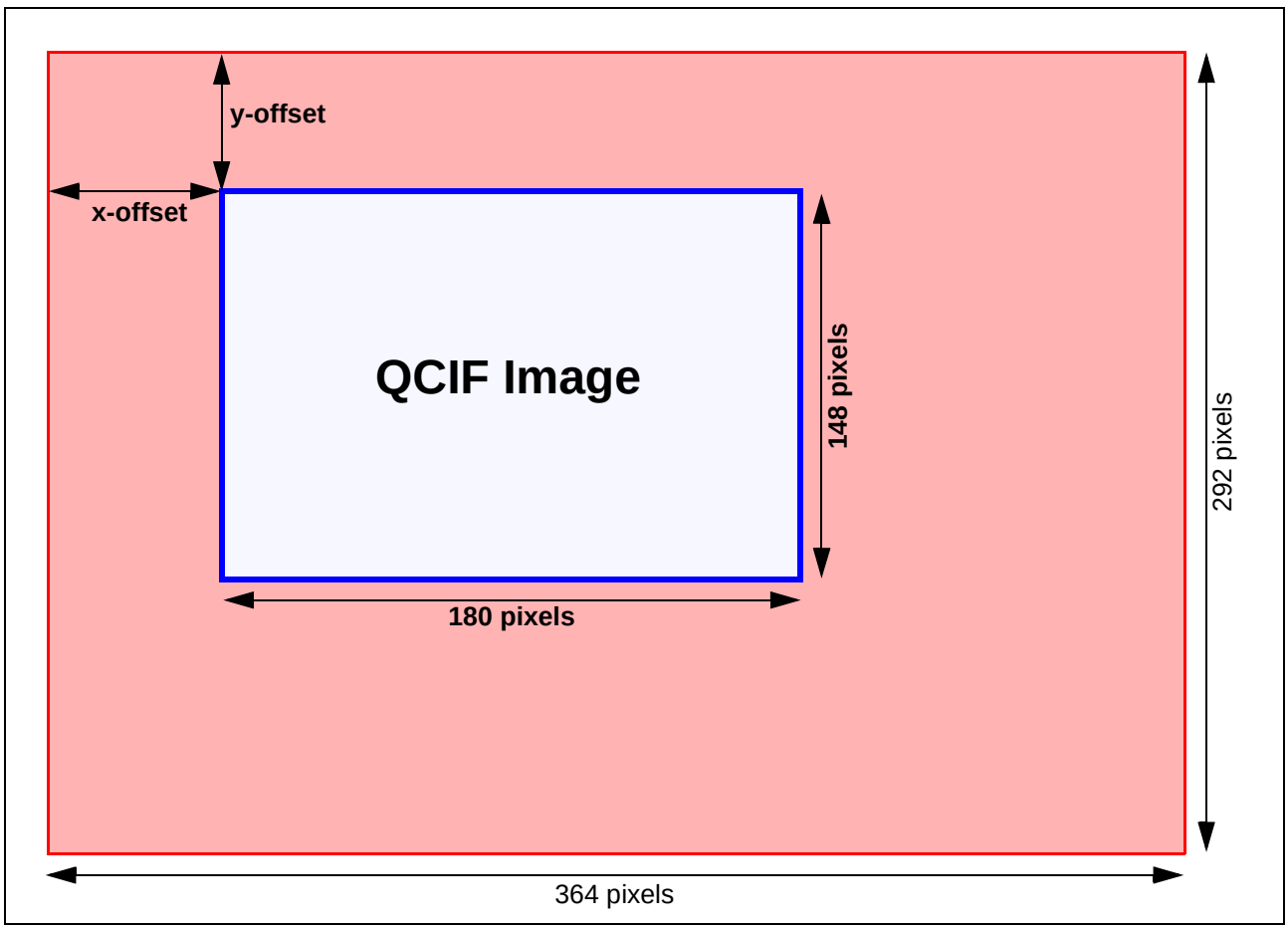
VV5411/VV6411 sensors have two QCIF resolution output modes, pan/tilt QCIF (ptQCIF) mode and sub sampled QCIF (ssQCIF) mode. The data contained within the QCIF window differs between the sub sampled and pan tilt modes. As the QCIF mode contains a quarter of the data of the CIF mode, the effective pixel clock can be run at a quarter of the rate. This means that in CIF mode, a system clock of 16MHz will produce a field rate of 30fps, whereas in QCIF mode a system clock of only 8MHz is required to produce the same field rate. Note that the sensor divides internally the system clock by 4 for CIF mode and by 8 for QCIF mode. If for example, the user supplies the sensor with a 16MHz system clock and selects the QCIF mode, the cresulting field rate of 60fps is available.

The QCIF output modes are targeted at applications where ultimate image resolution is not as important as perhaps limiting the data rate in a system or maximizing the frame rate for a given input clock rate.

2.4.1 Pan/Tilt QCIF

In this mode the QCIF image is generated by outputting a cropped portion of the CIF image as illustrated in *Figure 9*. When the pan-tilt QCIF video mode is initially selected, the image is horizontally and vertically justified within the full size array (364 pixels by 292 pixels). The coordinates defining the top left corner of the QCIF portion of the array to be output are defined by the x-offset & y-offset parameters in serial registers [88 - 91] inclusive.

Figure 9: Pan/Tilt QCIF image format



The x-offset and y-offset parameters are subject to minimum and maximum values which are set according to the video output mode/ and image processing effect (horizontal shuffle etc.) that have been selected. Any clipping (against a maximum) or clamping (against a minimum) are

automatically controlled by the sensor logic. Regardless of whether any of the shuffle/mirror modes have been selected, the user should always identify the top left corner coordinates as the x-offset and y-offset. To preserve the Bayer pattern at the sensor output, the first pixel image of the image should always be green followed by red. If the x or y offsets are adjusted by a single step, i.e. adjust the x-offset from n to n+1, then this pattern will be corrupted. The user should always write an **odd** number to the x and y offset registers to preserve the Bayer pattern. The VV5411 monochrome sensor is unaffected by such an adjustment of the x-offset coordinate, as the pixels do not include any color information.

2.4.2 Sub-sampled QCIF

In this mode the QCIF image is generated by sub-sampling the CIF image in groups of 4 pixels (in a 2 by 2 pattern). The Bayer pattern is preserved by skipping a column as illustrated in *Figure 10*. Although the former would not necessarily apply to a monochrome sensor, the same address sequence is preserved. VV5411 users should ignore the color references in *Figure 10*. Due to the crude nature of the sub-sampling, the resulting output image is of inferior quality but contains full field of view and is intended for gesture recognition applications or perhaps as a preview option before switching to pan tilt QCIF mode (and view the scene with more details).

Figure 10: Sub-sampled QCIF image format

Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green
Green	Red	Green	Red	Green	Red	Green	Red	Green	Red	Green	Red
Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green	Blue	Green

Bayer colorized pixel array

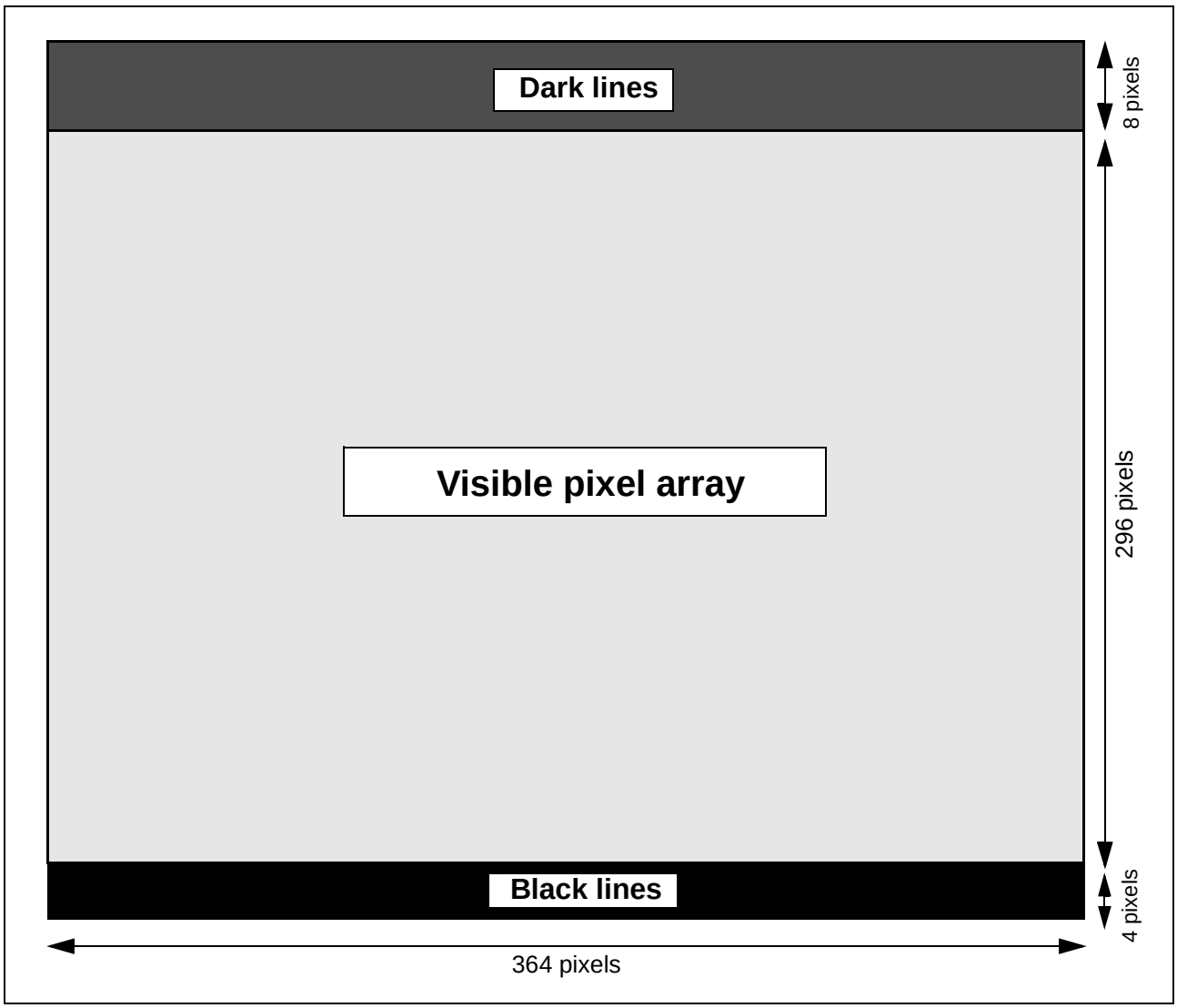
Green	Red			Green	Red			Green	Red		
Blue	Green			Blue	Green			Blue	Green		
Green	Red			Green	Red			Green	Red		
Blue	Green			Blue	Green			Blue	Green		

Sub-sampled Bayer colorized pixel array

3 Black Offset Cancellation

In order to produce a high quality output image from VV6411 it is important to maximize the dynamic range of the video output. This is achieved by accurately controlling the video signal black level. Within the sensor array of VV6411, there are a number of lines that are specified to be black, that is they are exposed to the incident light but they are always held in minimum exposure. VV6411 also has a number of dark lines, that is lines that are integrated for the same length of time as the visible lines but the pixels within these dark lines are shielded from incident light by an opaque material (e.g. metal 3). The *Figure 11* shows the location of the different types of lines within the full array.

Figure 11: Physical position of black and dark lines



VV5411/VV6411 can perform automatic black offset cancellation. VV5411/VV6411 contains an algorithm that monitors the level of the designated black pixels and applies a correction factor, if required, to provide an ideal black level for the video stream.

The user can control the application of the offset cancellation parameter. The internally calculated offset can be applied to the video stream or alternatively an externally calculated offset can be applied or finally there is the option of applying no offset at all. Details of how to select the afore-mentioned modes are given in Section 8.2.8.

The black offset cancellation algorithm accumulates data from the centre 2 of the 4 physical black lines. The internal cancellation algorithm uses a leaky integrator model to control the size of the calculated offset. The leaky integrator model uses the current offset plus a shifted version of the error between the ideal black level and the current offset as input. The shift magnitude in the error is programmable. It is also possible to control the range of pixel values that will inhibit a change in the calculated offset. A narrow band (128 +/- 2 codes) or a wide band (128 +/- 4 codes) can be selected. If the latter is selected and the pixel average returned in the current field lies between 124 and 132 then the offset cancellation remains unchanged.

Following a gain change, or when exiting low-power, sleep or suspend modes, the internal (19bit) offset register is reset to the default value, resulting in an automatic black offset of -64.

4 Dark Offset Cancellation

VV5411/VV6411 performs dark line offset cancellation as well as black line offset cancellation. A dark line is shielded from incident light by an opaque material such as metal 3 (as an example) but these lines will be exposed to incident light for the same length of time as the visible pixels. If the dark pixels are completely shielded from light, then no incident light should reach them so that they produce the same digital code as the black pixels, 64 in 10bit space. The algorithm used to calculate the dark offset cancellation is identical to the one used to calculate the black offset cancellation, however the dark algorithm does assume that the dark pixels have already been black-corrected. Therefore the target dark average is 64, thus the dark offset cancellation is 0 by default.

The dark offset cancellation algorithm is configured by the dark offset cancellation setup register, [46], see Section 8.2.6. The only parameter differing from the corresponding table that configures the black offset cancellation algorithm is the control bit, [bit2], that determines the number of dark lines used by the cancellation algorithm. It is possible to select half of the total number of available dark lines to be used to calculate the dark offset cancellation setting. When the former is selected, the dark lines used by the algorithm are always preceded by another dark line, thereby giving extra immunity from noisy edge effects that may occur on pixels close to the edge of the shield material.

It should be noted that the black and dark offset cancellation are completely independent. For example it is possible for the user to select internal automatic black offset cancellation but to opt for no dark offset cancellation or indeed choose to perform the dark offset cancellation externally.

5 Exposure Control

5.1 Calculating exposure period

The exposure time, comprising coarse and fine components, for a pixel and the analogue gain are programmable via the I^2C interface.

The coarse exposure value sets the number of complete lines a pixel exposes for, while the fine exposure sets the number of additional pixel clock cycles a pixel integrates for. The sum of the two gives the overall exposure time for the pixel array.

Exposure Time = ((Coarse setting x Line Period) + (Fine setting)) x (CLKI clock period) x Clock Divider Ratio (*Note 1*)

Note 1 *Clock Divider Ratio = 1/(Basic Clock Division * Optional Pixel Clock Divisor)*

Default Clock Divider Ratio as follows: (Optional Pixel Clock Divisor = 1)

- PAL/NTSC - 1/2
- CIF - 1/4
- QCIF - 1/8

The maximum coarse and fine exposure settings are a function of the field and line lengths respectively. The maximum coarse exposure is current field length - 2 and the maximum fine exposure is current line length - fixed offset. If a requested exposure value is beyond the maximum then the applied exposure setting will be clipped to the current maximum.

Table 6: Fine exposure offset

Video Mode	Fine Exposure Offset (pck's)
NTSC	51
PAL	86
CIF	51
QCIF	23

5.2 Gain components

The analogue gain in VV5411/VV6411 is programmed via the 8 bit gain register[36]. The analogue gain comprises 2 components: capacitive gain (set by the ms nibble), and current gain (set by the ls nibble). It is strongly recommended that the capacitive gain setting is left at the default value of 4'b1111. *Table 7* details the available gain settings in 9bit, (PAL or NTSC), and 10bit, (CIF or QCIF), modes. We assume that mode_select[24], bit1 is 0. gain[7:0] is the value programmed in register[36]. The ls nibble of the gain value is limited to 4'he, with 4'hf not permitted.

Table 7: Analogue gain settings

gain[7:0]	System Gain
8'hfc	4.000
8'hfb	3.200
8'hfa	2.667
8'hf9	2.2857
8'hf8	2.0000
8'hf7	1.7778
8'hf6	1.6000
8'hf5	1.4545
8'hf4	1.3333
8'hf3	1.2308
8'hf2	1.1429
8'hf1	1.0667
8'hf0	1.0000

5.2.1 Recommended gain settings

To ensure optimum sensor performance, it is recommended that the gain setting, controlled by the ls nibble of serial register[36_{10}], is limited to 12.

5.3 Clock division

Although the clock divisor register is an 8 bit register, the user only has write access to the 4 lower bits as described above. The 4 upper bits of the register are altered automatically when the video mode is changed by writing to Setup0[16] register. The 4 upper bits are pre-programmed as follows:

Table 8: System clock divisor options

Video mode	Register[37], bits[7:4]	Effective system clock divisor
CIF	4'b0001	Divide CLKI/CLKIP by 4
QCIF	4'b0011	Divide CLKI/CLKIP by 8
PAL/NTSC	4'b0000	Divide CLKI/CLKIP by 2

5.4 Updating exposure, gain and clock division settings

Although the user can write a new exposure, gain or clock division parameter at any point within the field, the sensor will only consume these new external values at a certain point. Exceptions to this behavior are when the user has selected immediate update of gain and clock division. In this particular case, the new gain or clock division value are applied as soon as the I^2C message has been completed. The fine and coarse exposure values are always written in a “timed” manner. There are a number of “update pending” flags available to the user (see Status0 reg[2] for details) with which the user can detect when the sensor has consumed one of the timed parameters. In the next section of this document, we detail all the timed parameters and describe when they are updated.

It is important to realize that there is a 1 frame latency between the moment when a new exposure value is applied to the sensor array and the moment when this new exposure value is read-out. The same latency does not exist for the gain value. To ensure that the effect of the new exposure and gain values are coincident, the sensor delays the application of the new gain value by approximately one frame relative to the application of the new exposure value.

If the user uses the auto increment option in the I^2C when writing a new series of exposure/gain and clock division parameters, it is important to ensure that the sensor receives the complete message bunch before starting to update any of the parameters. It is also important that the timed parameters are updated in the correct order, we will discuss this fully in the next section. If an auto increment message sequence is in progress but we have reached the point in the field timing where the gain value would normally be updated, we actually inhibit the update. Thus, we ensure that the gain change is not applied to the sensor while a change in the exposure is still pending.

6 Timed I²C Parameters

In *Chapter 5: Exposure Control on page 25*, we introduced the concept of “timed parameter”, an information that is written via the I²C but is not used immediately by the sensor. There is a delay before the information is passed to the internal registers (also referred to as working registers) from the I²C registers (also referred to as shadow registers). The working registers content determines the sensor behavior.

The VV5411/6411 architecture requires that many of the programmable registers are handled this way. This chapter describes these registers, their use and update.

6.1 Listing and categorizing the parameters

The timed parameters are split into 6 categories as listed here below:

- fine exposure
- coarse exposure
- clock division
- gain
- pan parameter
- tilt parameter
- video timing

There is a “pending” flag for each of the above categories. These flags are stored in Status0 Register[2]. High flags indicate that the related working registers need updating from the according shadow registers. This feedback information is useful if for example, a user attempts to write an exposure controller. The status of the pending flags allows accurate timing of the I²C communications.

6.1.1 Fine exposure

The fine exposure category simply comprises registers[32,33].

6.1.2 Coarse exposure

The coarse exposure category simply comprises registers[34,35].

6.1.3 Clock division

The clock division category simply comprises register[37].

6.1.4 Gain

The gain category simply comprises register[36].

6.1.5 Pan parameter

The pan parameter category comprises the following registers:

- Setup0[16] (“pan_pend” flag only set if the subsampled QCIF mode is entered or exited)
- Setup1[17] (“pan_pend” flag only set if the hshuffle control bit is in changing state)
- Data_format[22] (“pan_pend” flag only set if the hmirror control bit is in changing state)
- X-offset[87,88] (“pan_pend” flag set unconditionally)

6.1.6 Tilt parameter

The tilt parameter category comprises the following registers:

- Setup0[16] (“tilt_pend” flag only set if the subsampled QCIF mode is entered or exited)
- data_format[22] (“tilt_pend” flag set if the hshuffle control bit or the hmirror control bit is in changing state)
- Y-offset[89,90] (“tilt_pend” flag set unconditionally)

6.1.7 Video timing parameter

The video timing parameter category includes all the other shadow/working register pairs. The pending flag for the video timing parameter update is unconditionally set if any of the following registers are written to:

- Setup0[16]
- Setup1[17]
- fg_mode[20]
- data_format[22]
- op_format[23]
- mode_select[24]
- Dark Pixel Offset[44,45]
- Dark Pixel Cancellation Setup Register
- Black Pixel Offset[44,45]
- Black Pixel Cancellation Setup Register
- Line Length[82,83]
- Field Length[97,98]

6.2 Timed parameter update points

The timed parameter categories are updated as follows:

Note: We refer to odd and even fields in the following Table 9 because in CIF or QCIF video modes all fields have identical length and consequently difficult to differentiate.

Table 9: Timed parameter update points

Timed parameter category	Updated point
Fine exposure	Conditional on a change pending in the line length register. ***Line length change pending***: update fine exposure at the odd to even field transition ***Line length change not pending***: update fine exposure during the start of active video (SAV) region of the end of frame (EOF) line (the line that follows the last line of active video) in the odd field.
Coarse exposure	Updated during the SAV region of the first dark line in an odd field
Clock division	Updated at the odd to even field transition
Gain	Updated during the SAV region of the EOF line in the odd field
Pan parameter	Updated during the SAV region of the EOF line in the odd field
Tilt parameter	Updated during the SAV region of the first visible line in an odd field
Video timing	Updated at the odd to even field transition

The order in which timed parameters are updated is critical. Assuming all pending flags are set (at least one register in each category), the working registers are updated in the following order:

1 Coarse exposure
2 Tilt parameters
3 Gain, Pan parameters and conditionally the fine exposure (*Table 9*)
4 Clock division, video timing parameters and conditionally the fine exposure (*Table 9*)

7 Digital Video Interface Format

7.1 General description

The video interface is a bidirectional, tri-stateable 5-wire data bus. The nibble transmission is synchronized with the rising edge of the system clock (*Figure 28*).

Table 10: Video encoding parameters

Read-out Order	Progressive scan (non-interlaced)			
Form of encoding	Uniformaly quantized, PCM, 8/10 bits per sample			
Relationship between video signal levels and quantisation levels	The internal10-bit pixel data is clipped to ensure that 0_H and $3FF_H$ (5-wire) or FF_H (4/8 -wire) values do not occur when pixel data is output on the data bus.			
	10-bit data		8-bit data	
	Pixel values	1 to 1022	Pixel values	1 to 254
	Black level	64	Black level	16

Digital video data which are either 8 or 10 bits per sample are transmitted in one of the following ways:

10-bit data

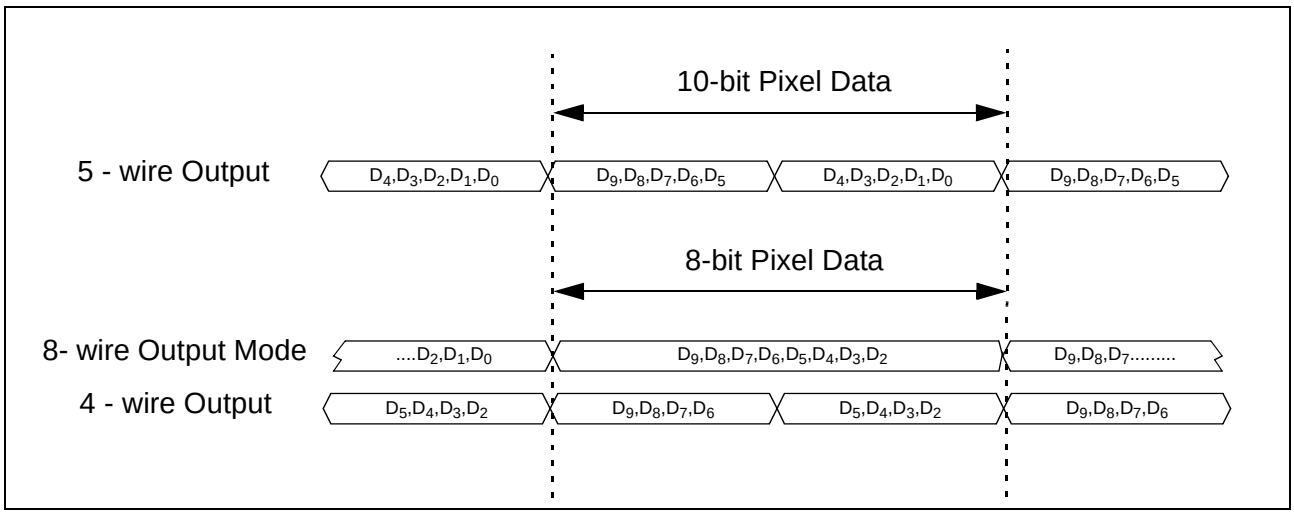
- one pair series of 5-bit nibbles, most significant nibble first, on 5 wires.
- One 8-bit number e.g. line code. line numbers and status line data is padded with 00 in the least significant two bits to make up a 10-bit value.

8-bit data

- A single 8 bit byte over 8 output wires (see *Note 1*).
- A series pair of 4-bit nibbles, most significant nibble first, on 4 wires.
- The top 8-bits of a 10-bit value e.g. pixel data or line averages is used as the 8-bit equivalent.

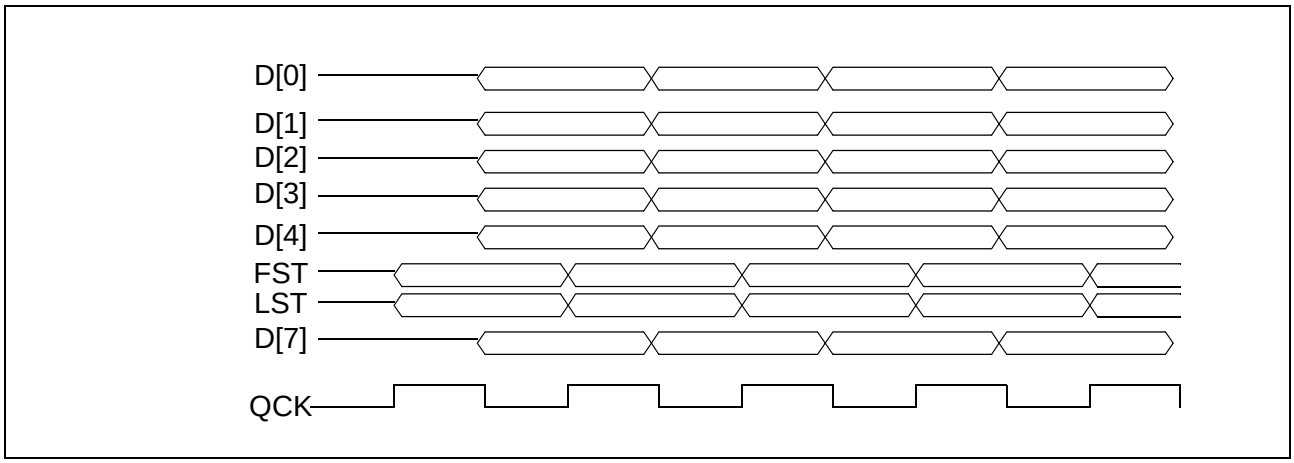
Note 1 if the 8-wire output mode is selected , the normal FST/LST pin function is sacrificed as these pins are required to output data information.

Figure 12: Possible output modes



In 8- wire output mode, data on FST and LST (bits D[5] and D[6]) are in advance by 1/2 qck cycle of bits D[0] to D[4] and D[7]. *Figure 13* shows the detailed timing in this mode.

Figure 13: 8-wire mode detailed timing



In the following description, the 4-wire mode is used as an example. The 5-wire mode can be viewed as a variant of the 4-wire mode. Data is output on the least significant data wires available: in 4-wire mode, data is output on data wires D[3:0] while in 5-wire mode data is output on D[4:0].

Multiplexed with the sampled pixel data is control information including both video timing references and sensor status/configuration data.

Video timing reference information takes the form of field start characters, line start characters, end of line characters and a line counter.

Where hexadecimal values are used, they are indicated by a subscript H, such as FF_H; other values are decimal.

7.1.1 Embedded control data

To distinguish between control data and sampled video data, all control data is encapsulated in embedded control sequences. These 6 bytes-long sequences include a combined escape/sync character sequence, 1 control byte (the ‘command byte’) and 2 bytes of supplementary data.

To minimize the susceptibility of the embedded control data to random bit errors, we used redundant coding techniques to correct single bit errors in the embedded control words. However, more serious corruption of control words or the corruption of escape/sync characters cannot be tolerated without loss of sync to the data stream. We devised a simple set of rules to ensure that a loss of sync is detected. The four exceptions to the rules are outlined her below:

- Data containing a command word with two bit errors.
- Data containing two ‘end of line’ codes not separated by a ‘start of line’ code.
- Data preceding an ‘end of field’ code before a start of frame’ code has been received.
- Data containing line that do not have sequential line numbers (excluding the ‘end of field’ line).

If the host detects one of these violations then it should abandon the current video field.

7.1.2 The combined escape and sync character

Each embedded control sequence begins with a combined escape and sync character made of three words. The first two words: FF_H FF_H- are illegal in normal data. The next word: 00_H guarantees a clear signal transition that allows a host to determine the position of the word

boundaries in the serial stream of nibbles. Combined escape and sync characters are always followed by a command byte - making up the four byte minimum embedded control sequence.

7.1.3 The command word

The byte that follows the combined escape/sync characters defines the type of embedded control data. Three of the 8 bits are used to carry the control information, four are 'parity bits' used by the host to detect and correct a certain level of errors in the transmission of the command words, the remaining bit is always set to 1 to ensure that the command word never has the value 00_H. The coding scheme used allows the correction of single bit errors (in the 8-bit sequence) and the detection of 2 bit errors The three data bits of the command word are interpreted as shown in *Figure 14*.The even parity bits are based on the following relationships:

- An even number of ones in the 4-bit sequence (C_2, C_1, C_0 and P_0).
- An even number of ones in the 3-bit sequence (C_2, C_1, P_1).
- An even number of ones in the 3-bit sequence (C_2, C_0, P_2).
- An even number of ones in the 3-bit sequence (C_1, C_0, P_3).

Table 11 shows how the parity bits are used to detect and correct 1-bit errors and detect 2-bit errors.

7.1.4 Supplementary data

The last 2 bytes of the embedded control sequence include supplementary data. There are two options:

- The last 2 bytes of the SAV 6-byte sequence contain the current 12-bit line number. The 12-bit line number is split into two 6-bit values. Each 6-bit value is then converted into an 8-bit value by adding a zero to the start and an odd word parity bit at the end.
- The 5th byte of the EAV sequence contains a pixel average for that line either based upon the middle 256 pixels in CIF,PAL or NTSC video modes, or the middle 128 pixels in QCIF video mode. The final byte is FF_H.

Note: in 5-wire mode, the embedded control data is calculated as detailed above and output as the most significant 8-bits. The least significant 2-bits are padded with zero.

Table 11: Embedded line codes

Line Code	Nibble X_H (1 C_2 C_1 C_0)	Nibble Y_H (P_3 P_2 P_1 P_0)
End of Line	1000_2 (8_H)	0000_2 (0_H)
Blank Line (BL)	1001_2 (9_H)	1101_2 (D_H)
Black line (BK)	1010_2 (A_H)	1011_2 (B_H)
Visible Line (VL)	1011_2 (B_H)	0110_2 (6_H)
Start of Even Field (SOEF)	1100_2 (C_H)	0111_2 (7_H)
End of Even Field (EOEF)	1101_2 (D_H)	1010_2 (A_H)
Start of Odd Field (SOOF)[a]	1110_2 (E_H)	1100_2 (C_H)
End of Odd Field (EOOF)[b]	1111_2 (F_H)	0001_2 (1_H)

a. This code is only generated in the PAL or NTSC video modes

b. This code is only generated in the PAL or NTSC video modes

We include *Table 12* to show how the 8 bit control codes are mapped onto the output data bits in the 5 wire mode.

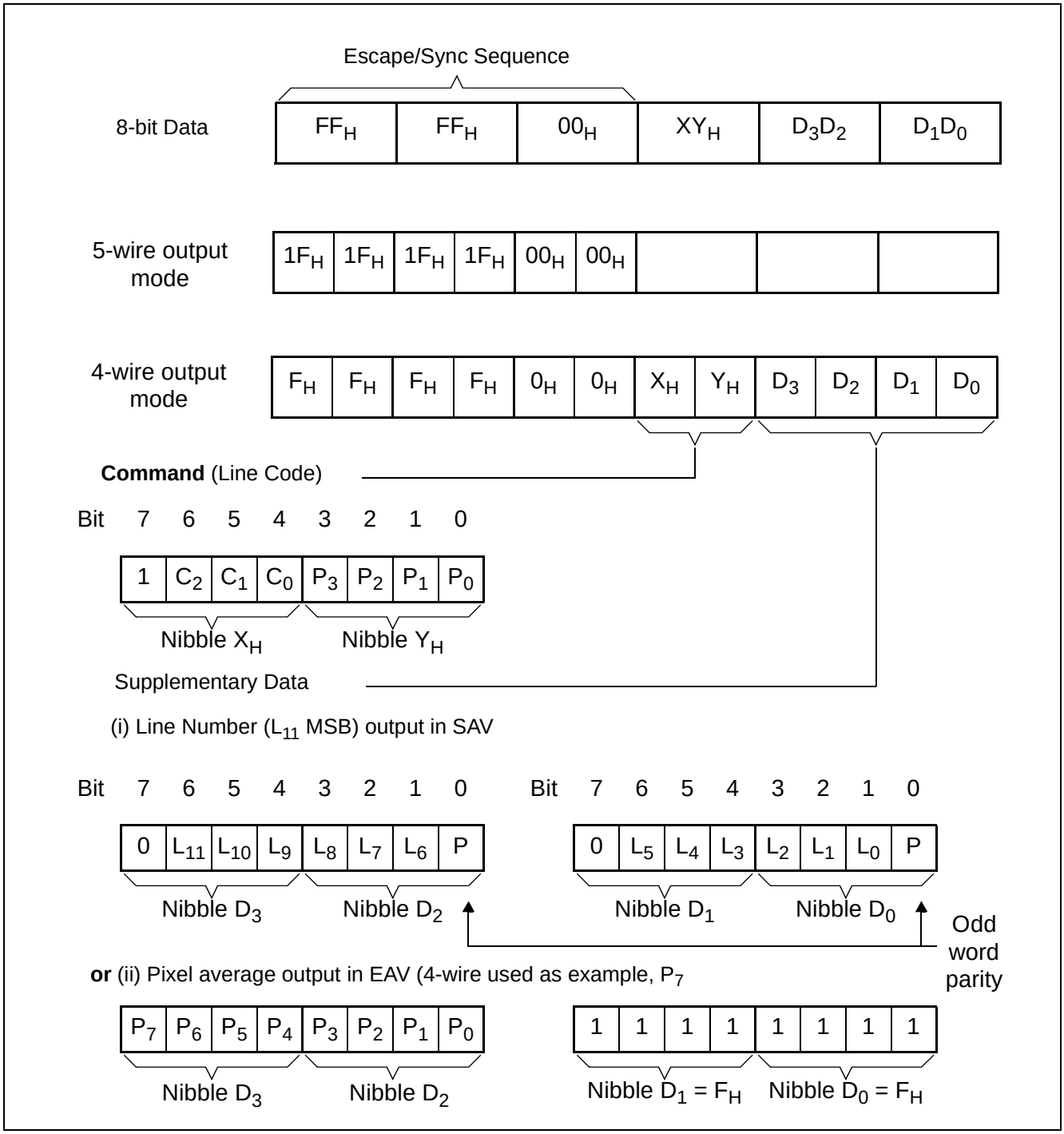
Table 12: Mapping 8bit control codes to 5 wire output mode

Line Code	Most significant nibble Data[4:0]	Least significant nibble Data[4:0]
End of Line	1_0000_2 (10_H)	0_0000_2 (00_H)
Blank Line (BL)	1_0011_2 (13_H)	1_0100_2 (14_H)
Black line (BK)	1_0101_2 (15_H)	0_1100_2 ($0C_H$)
Visible Line (VL)	1_0110_2 (16_H)	1_1000_2 (18_H)
Start of Even Field (SOEF)	1_1000_2 (18_H)	1_1100_2 ($1C_H$)
End of Even Field (EOEF)	1_1011_2 ($1B_H$)	0_1000_2 (08_H)
Start of Odd Field (SOOF)	1_1101_2 ($1D_H$)	1_0000_2 (10_H)
End of Odd Field (EOOF)	1_1110_2 ($1E_H$)	0_0100_2 (04_H)

Table 13: Parity checking

Parity Checks				Comment
P_3	P_2	P_1	P_0	
✔	✔	✔	✔	Code word un-corrupted
✔	✔	✔	✘	P_0 corrupted, line code OK
✔	✔	✘	✔	P_1 corrupted, line code OK
✔	✘	✔	✔	P_2 corrupted, line code OK
✘	✔	✔	✔	P_3 corrupted, line code OK
✘	✘	✔	✘	C_0 corrupted, invert sense of C_0
✘	✔	✘	✘	C_1 corrupted, invert sense of C_1
✔	✔	✘	✘	C_2 corrupted, invert sense of C_2
All other codes				2-bit error in code word.

Figure 14: Embedded control sequence



7.2 Video timing reference and status/configuration data

Each video sequence frame comprises 2 fields. Each data field is built with the following sequence of data lines.

- A start of field line
- A number of black lines
- A number of blank (or dark) lines
- A number of active video lines
- An end of field line
- A number of blank or black lines

Table 14: Field and frame formats

Video Format	NTSC			PAL			CIF			QCIF		
VP3 mode	On		Off	On		Off	On		Off	On		Off
Extra Black Lines	On	Off	N/A	On	Off	N/A	On	Off	N/A	On	Off	N/A
1st field												
Start of field line	1	1	1	1	1	1	1	1	1	1	1	1
Black lines	8	2	8	8	2	16	8	2	16	8	2	8
Blanking lines	1	7	0	1	7	0	1	7	0	1	7	0
Dark lines	0	0	8	0	0	2	0	0	10	0	0	2
Active video lines	244	244	244	292	292	292	292	292	292	148	148	148
End of field line	1	1	1	1	1	1	1	1	1	1	1	1
Blanking lines	0	7	0	0	9	0	0	17	0	0	1	0
Black lines	7	0	0	9	0	0	17	0	0	1	0	0
Total	262	262	262	312	312	312	320	320	320	160	160	160
2nd field												
Start of field line	1	1	1	1	1	1	1	1	1	1	1	1
Black lines	8	2	8	8	2	16	8	2	16	8	2	8
Blanking lines	1	7	0	1	7	0	1	7	0	1	7	0
Dark lines	0	0	8	0	0	2	0	0	10	0	0	2
Active video lines	244	244	244	292	292	292	292	292	292	148	148	148
End of field line	1	1	1	1	1	1	1	1	1	1	1	1
Blanking lines	0	8	0	0	10	0	0	17	0	0	1	0
Black lines	8	0	1	10	0	1	17	0	0	1	0	0
Total	263	263	263	313	313	313	320	320	320	160	160	160

Table 14 details the number of each type of data lines for NTSC, PAL, CIF and QCIF output formats. Each line of data starts with an embedded control sequence that identifies the line type (as outlined in *Table 14*). The control sequence is then followed by two bytes that contain a coded line number. The line number sequences starts with the start-of-frame line at 00_H and increments one per line up until the end-of-frame line. Each line is terminated with an end-of-line embedded control sequence.

The line start embedded sequences are used to recognize visible video lines and avoid that a number of null bytes are inserted between successive data lines.

The following series of figures (*Figure 15* ->*Figure 26*) show line type construction of the fields in each of the available video modes for the VV5411/VV6411.

7.2.1 Blank lines

In addition to padding between data lines, actual blank data lines may appear in the positions indicated above. These lines begin with start-of-blank-line embedded control sequences and are constructed identically to active video lines except that they only contain blank bytes, 07_H, (expressed as $01C_H$ in 10bit form).

7.2.2 Black line timing

The black lines (which are used for black offset calculation) are identical in structure to valid video lines except that they begin with a start-of-black line code and contain either information from the sensor black lines or blanking data.

By default VP3 mode (see mode_select[24] for details) is selected. It is an option in any of the VP3 modes to select the additional black lines to be output (line 3-8). If the VP3 mode is not selected then all the black lines are enabled - no blank lines are output.

The concept of dark lines which is internal, is used for dark offset cancellation (see following diagrams to identify their position within the frame timing model), however the dark lines share the same line type code as the black lines externally.

7.2.3 Padding lines and fields

The user may choose to extend the inter-field period by increasing the field length by writing to serial registers 97 & 98. In this event, the appropriate number of additional black or blank lines is inserted between the End Of Field (EOF) line and the Start Of Field (SOF) line. This means that the distance between SOF and EOF remains constant.

The user can also extend the line length by writing to serial registers 82 and 83. The line length padding is inserted after the EAV sequence, ensuring that the distance between the SAV and EAV sequences remains constant.

7.2.4 Fields and frames

Although we use the terms of ‘fields’ and ‘frames’, they do not have the conventional meaning normally associated with them. The PAL and NTSC video modes have frames of 625 and 525 lines respectively. However, the individual fields do not contain the normal half line detail, rather the first field is a full line shorter than the second field in the frame. Therefore the PAL frame is composed of 2 fields, the first being 312 lines long and the second being 313 lines long. Note that the number of active video lines is the same for both fields.

The internal video timing engine also requires a ‘2 field to a frame’ concept as specific events are triggered at a frame rate rather than field rate.

Figure 15: NTSC field and frame formats - VP3 mode on, extra-black lines off

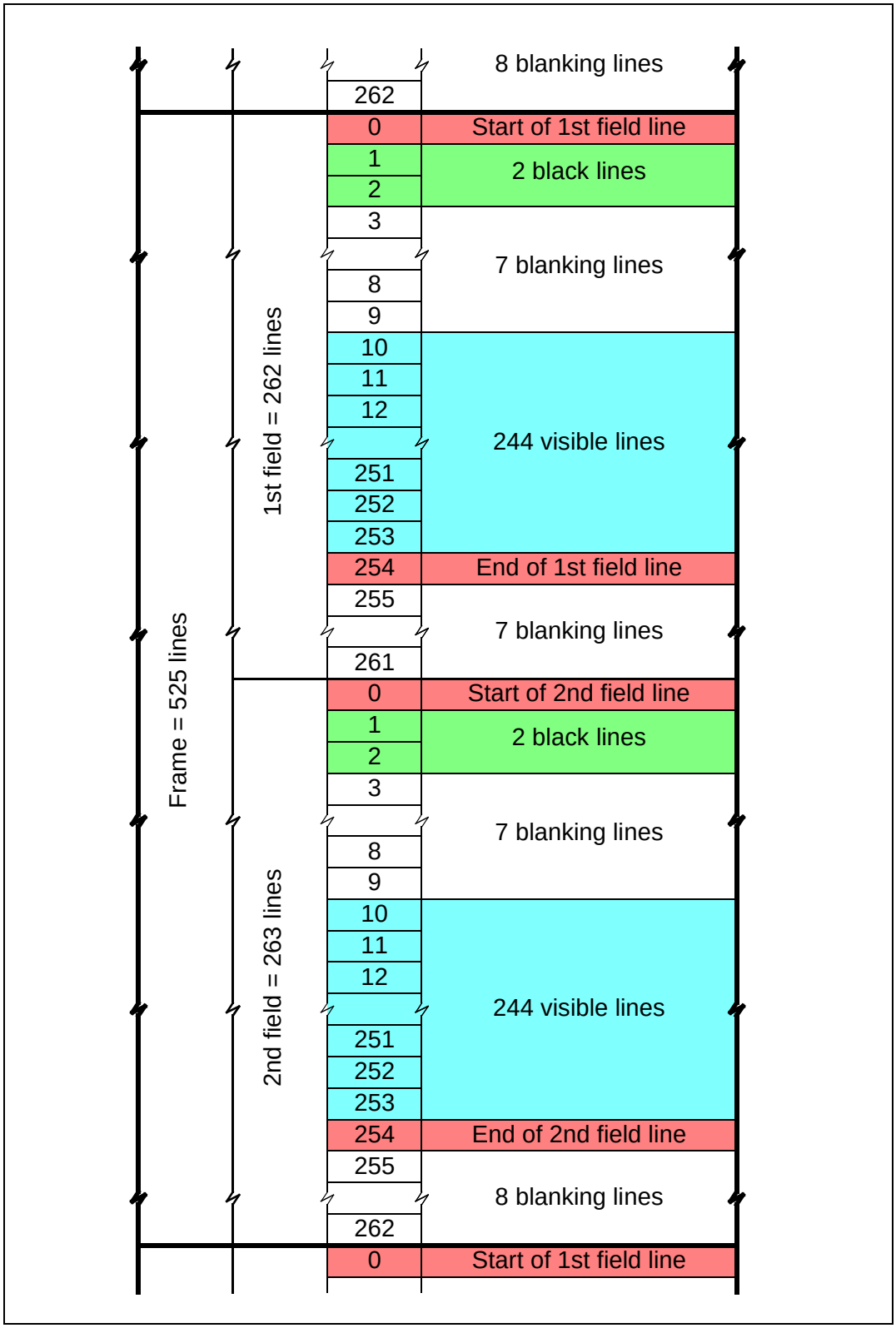


Figure 16: NTSC field and frame formats - VP3 mode on, extra black lines on

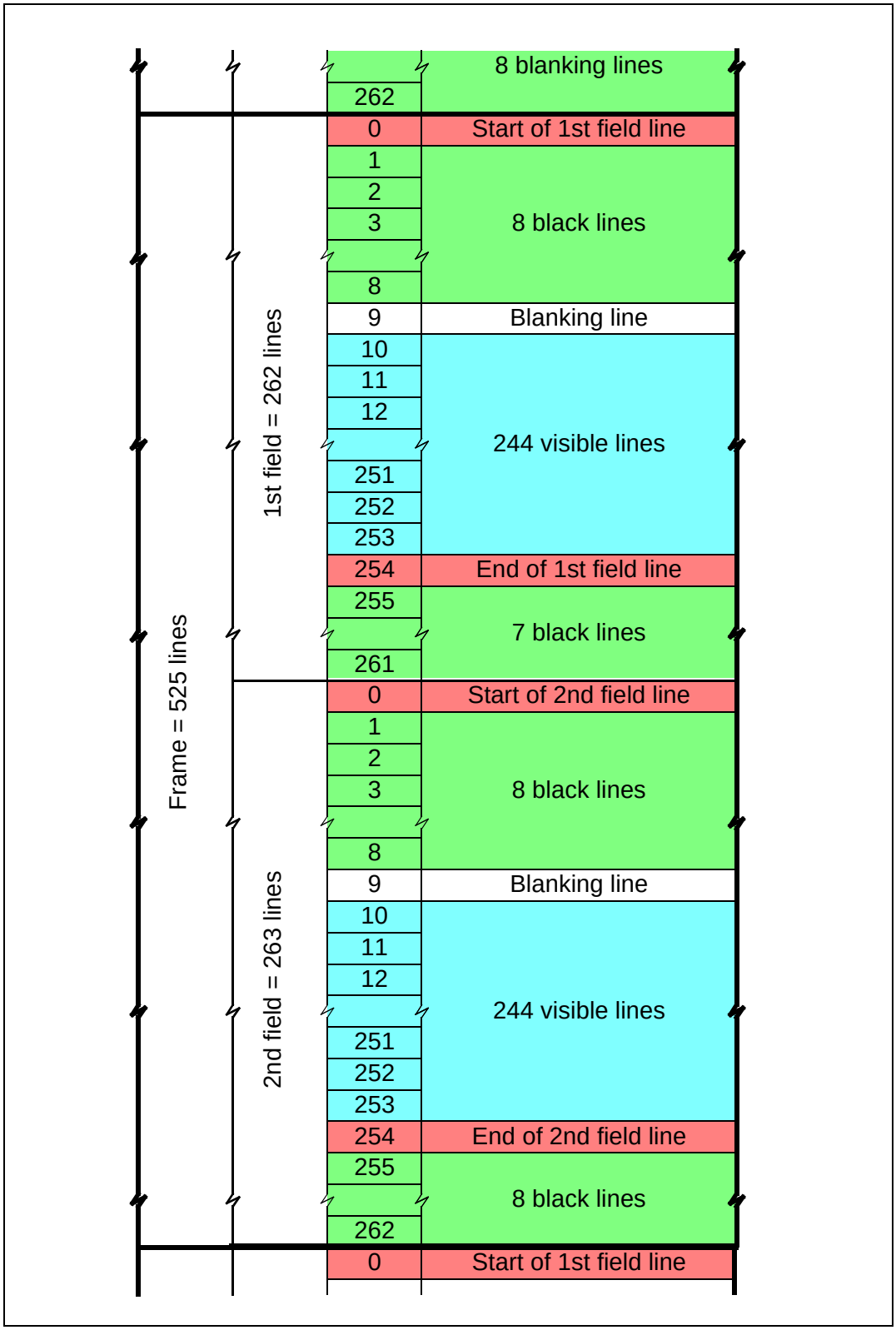


Figure 17: NTSC field and frame formats - VP3 mode off

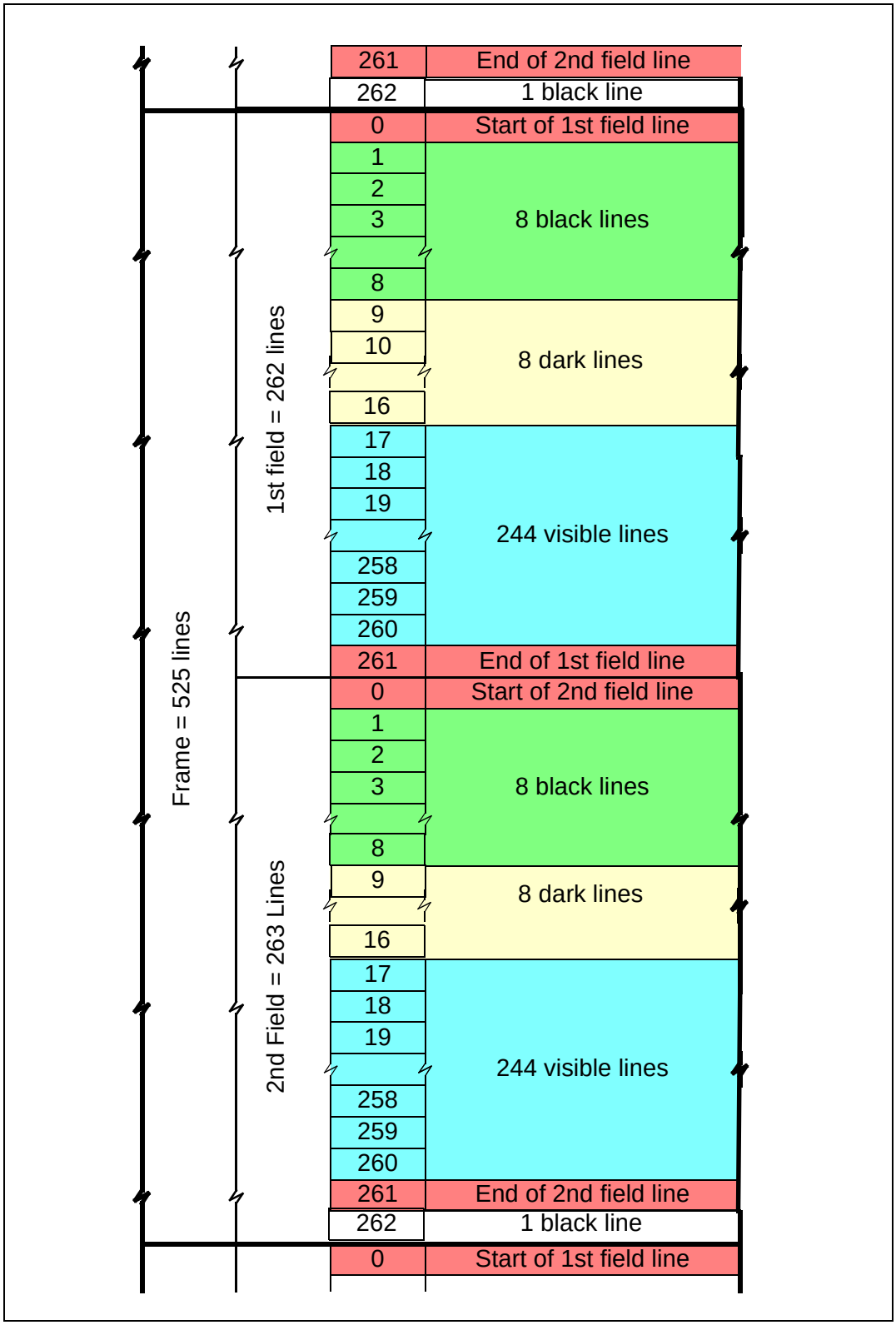


Figure 18: PAL field and frame formats - VP3 mode on, extra black lines off

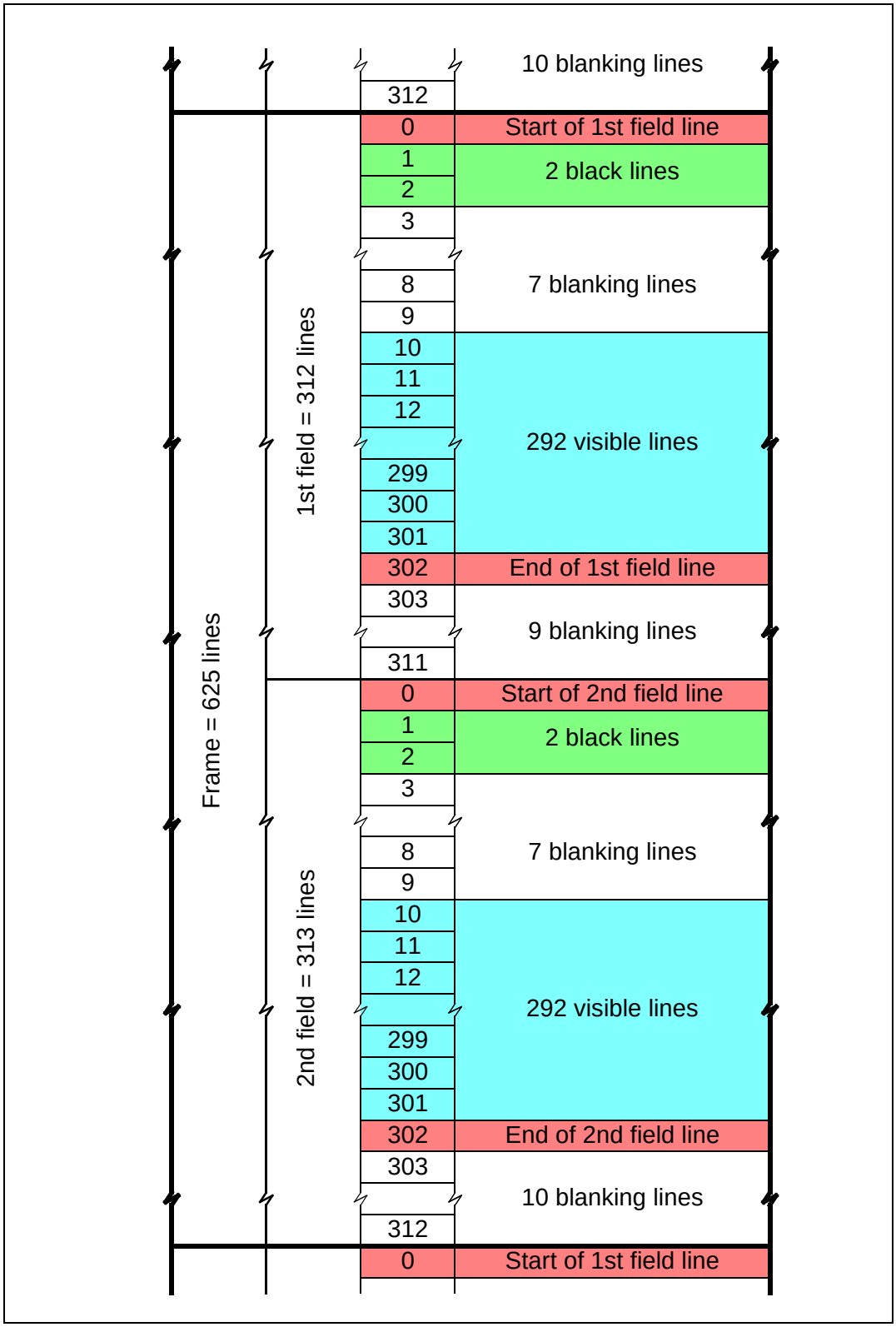


Figure 19: PAL field and frame formats - VP3 mode on, extra black lines on

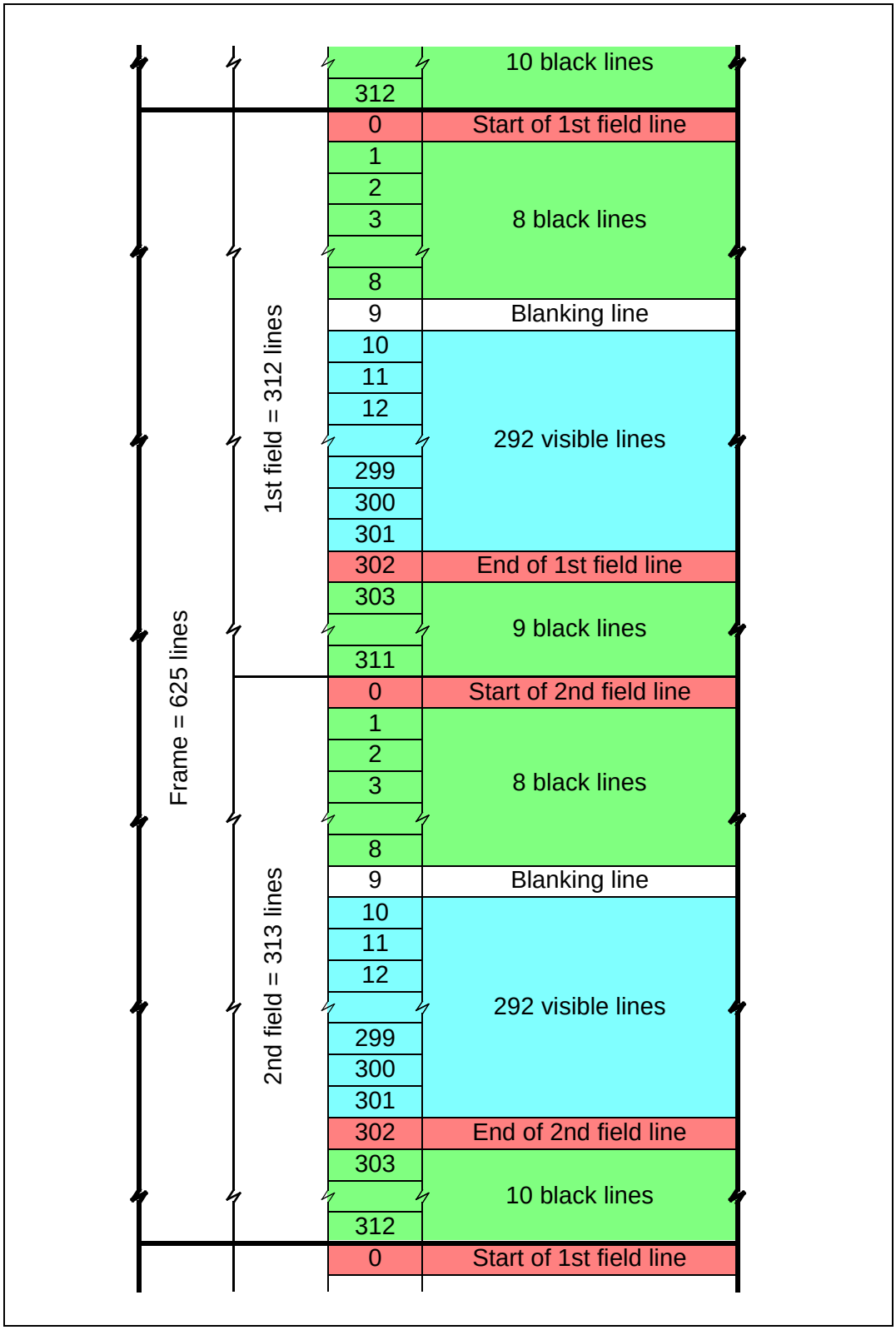


Figure 20: PAL field and frame formats - VP3 mode off

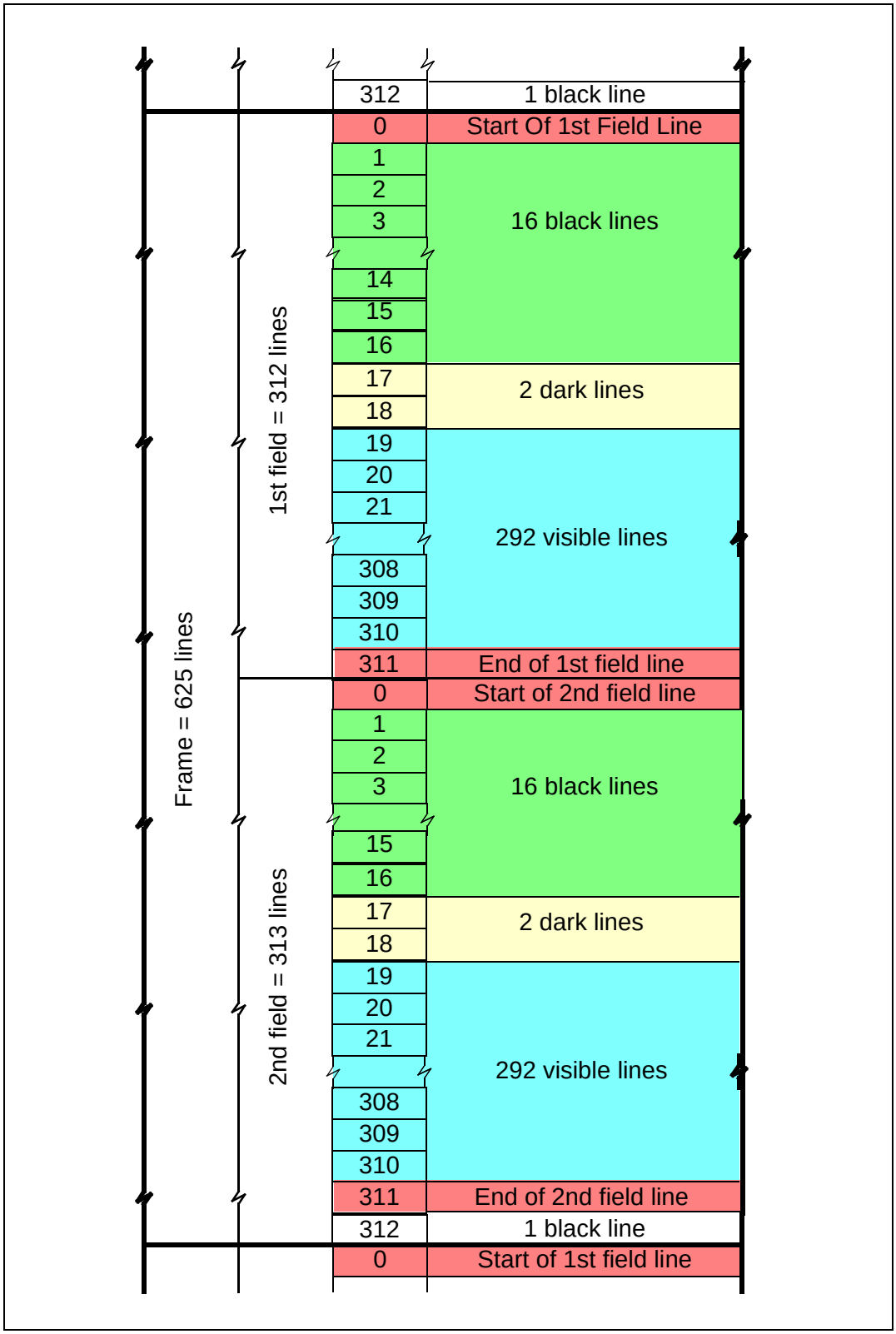


Figure 21: CIF field and frame formats - VP3 mode on, extra black lines off

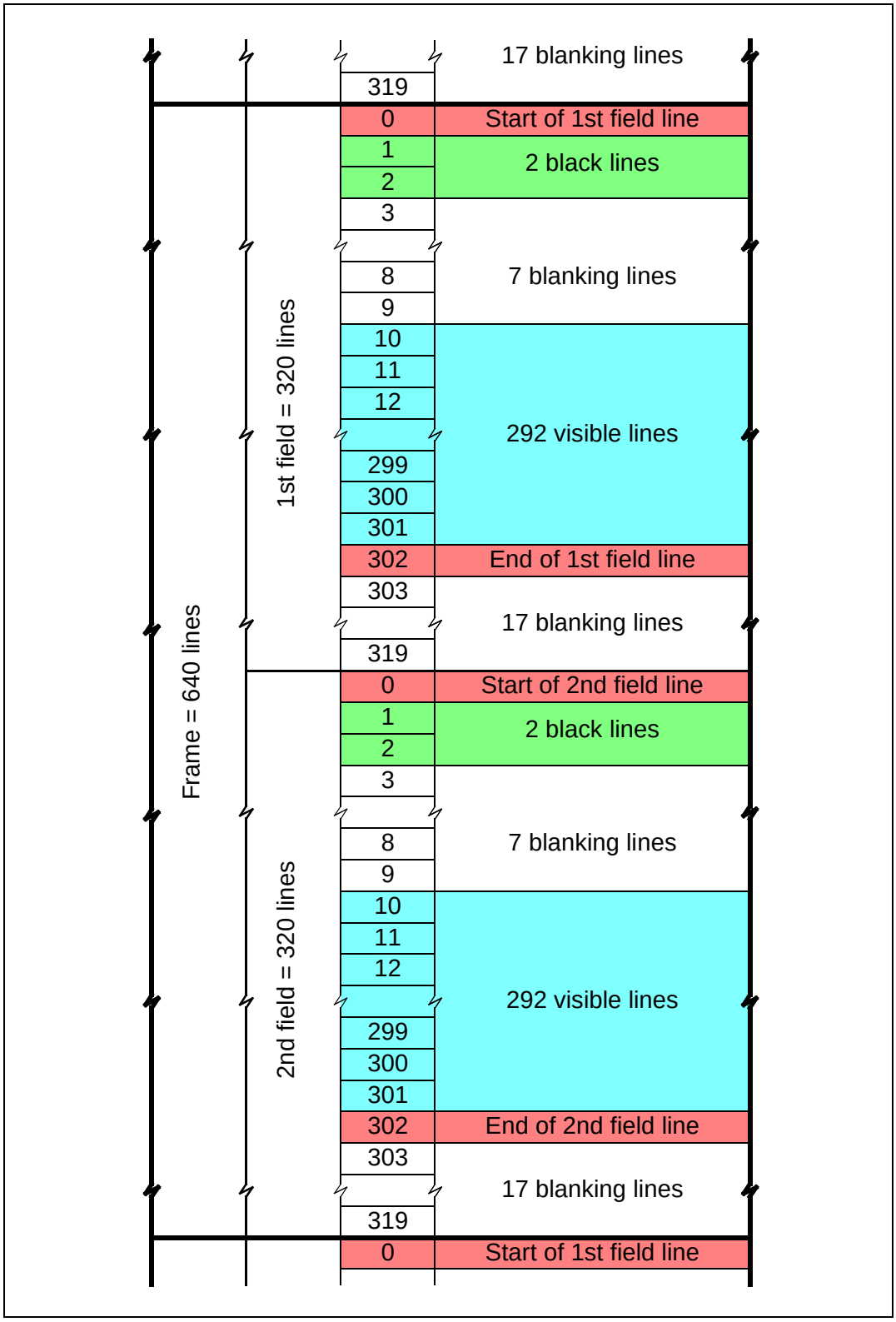


Figure 22: CIF field and frame formats - VP3 mode on, extra black lines on

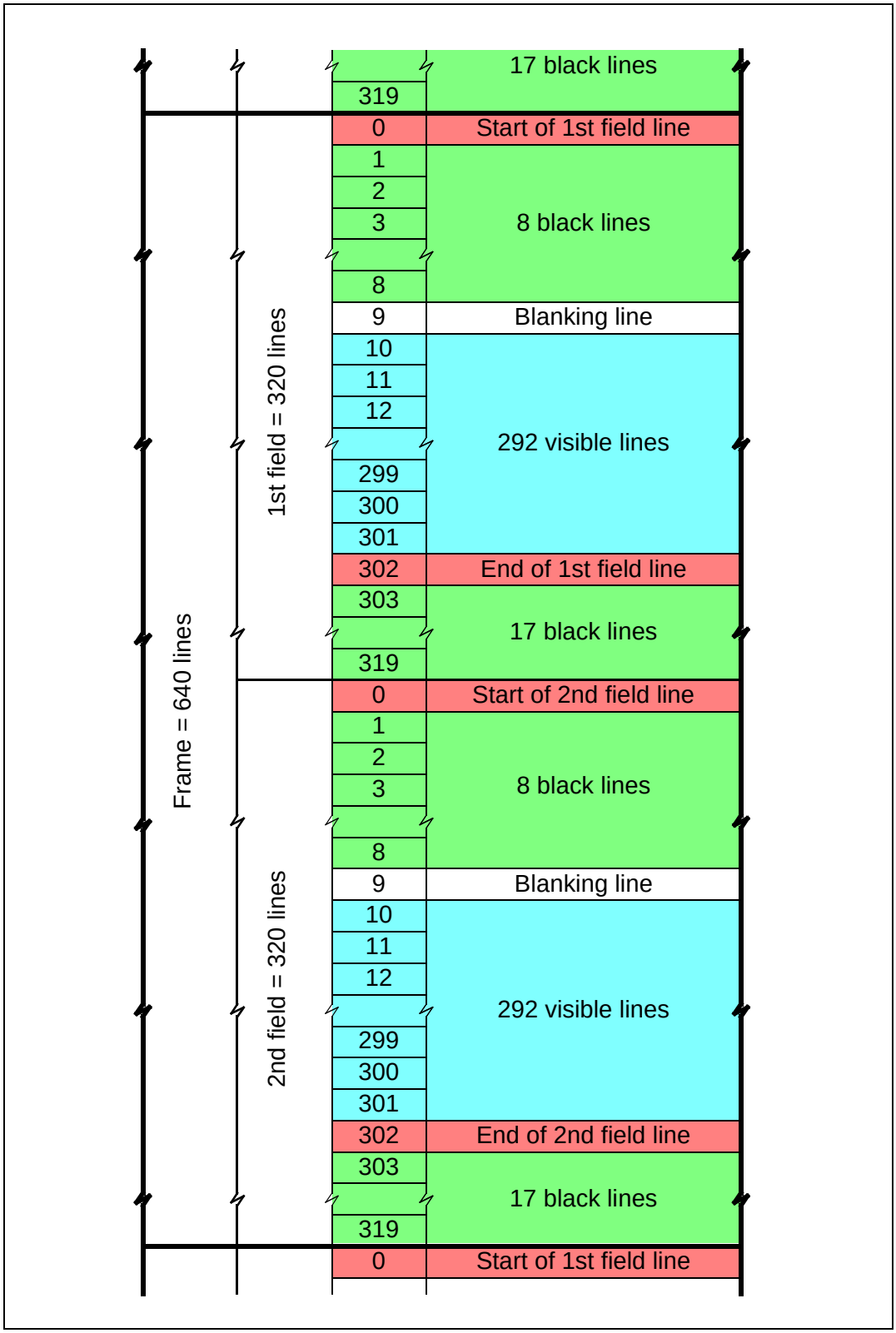


Figure 23: CIF field and frame formats - VP3 mode off

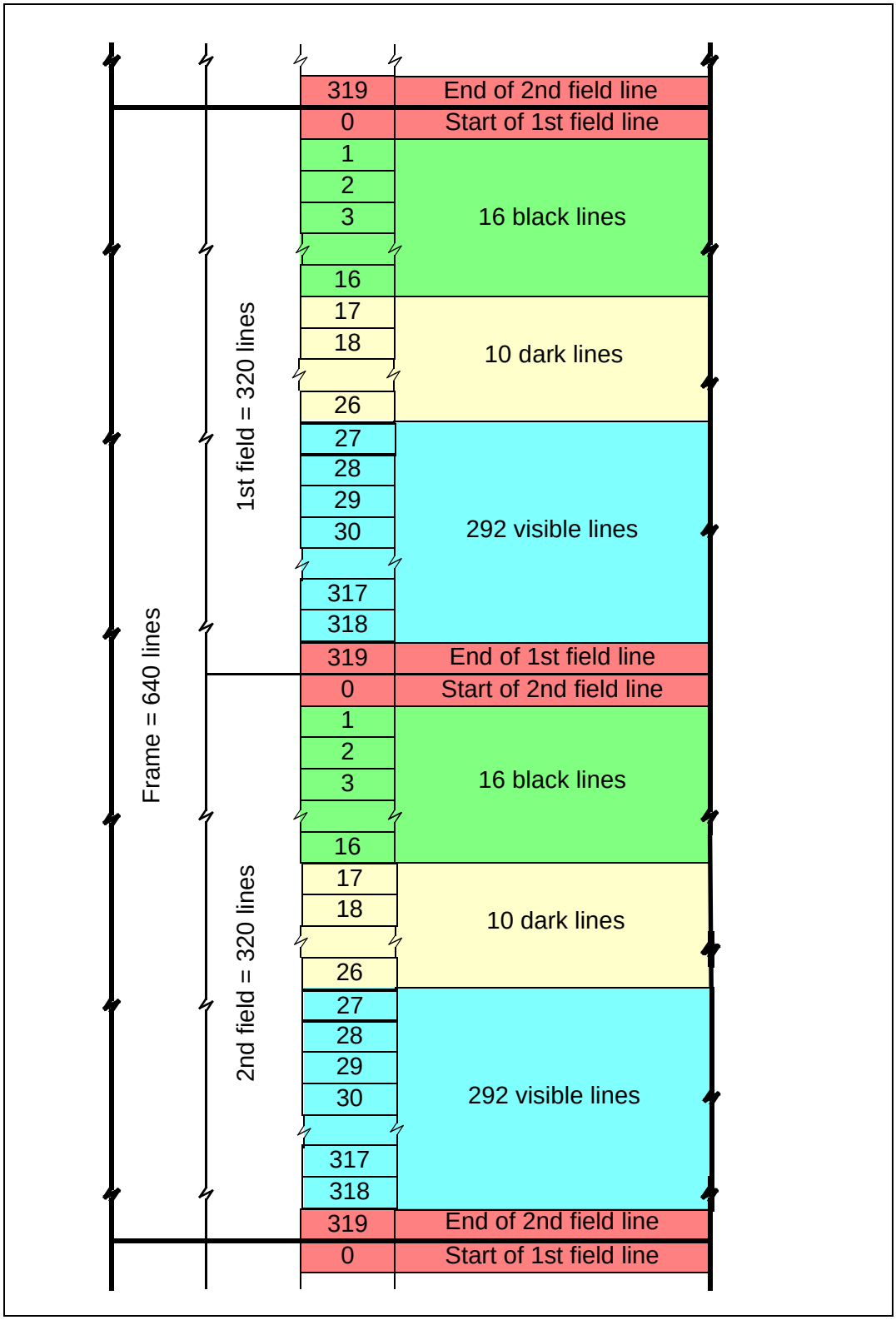


Figure 24: QCIF field and frame formats - VP3 mode on, extra black lines off

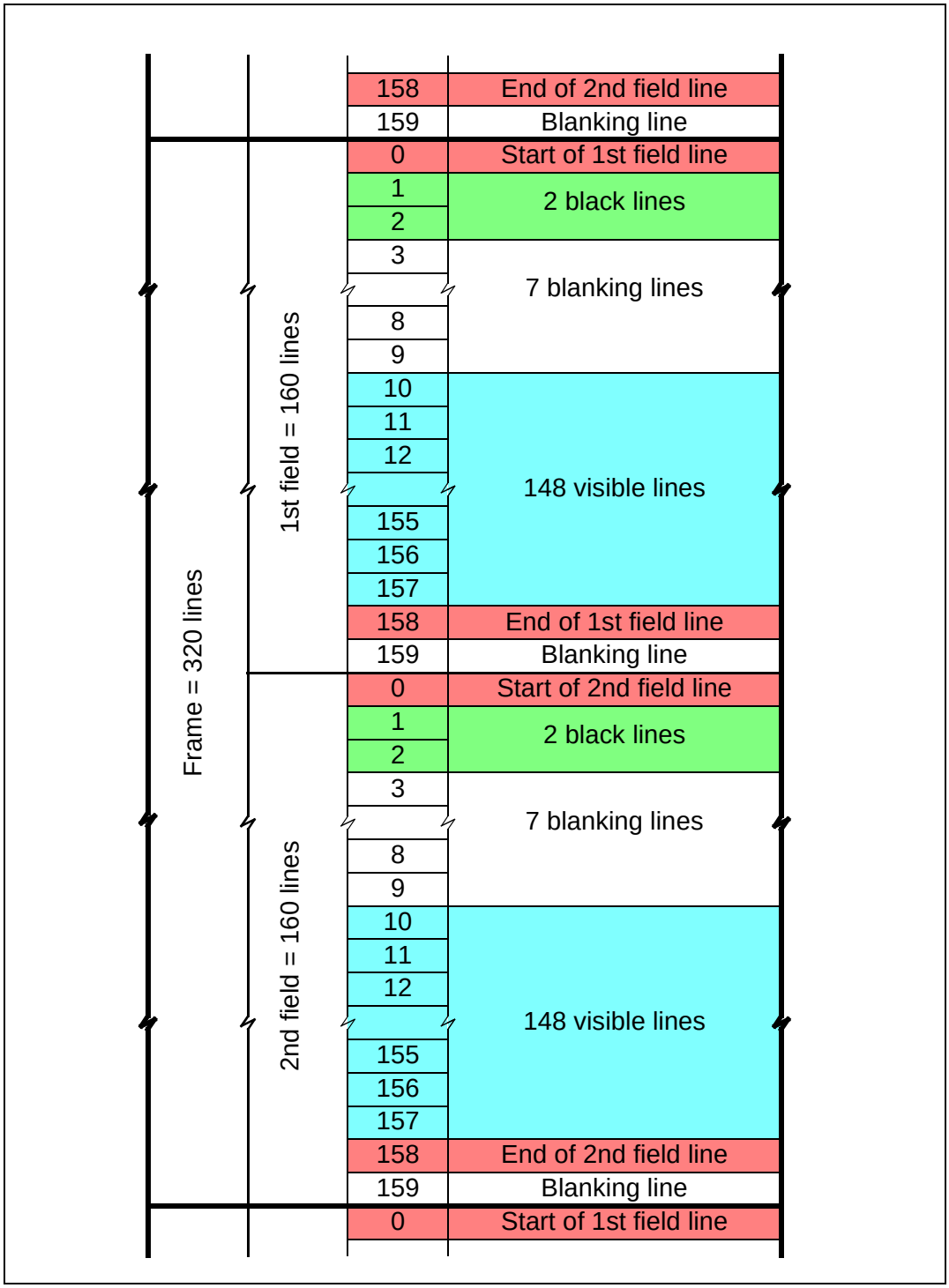


Figure 25: QCIF field and frame formats - VP3 mode on, extra black lines on

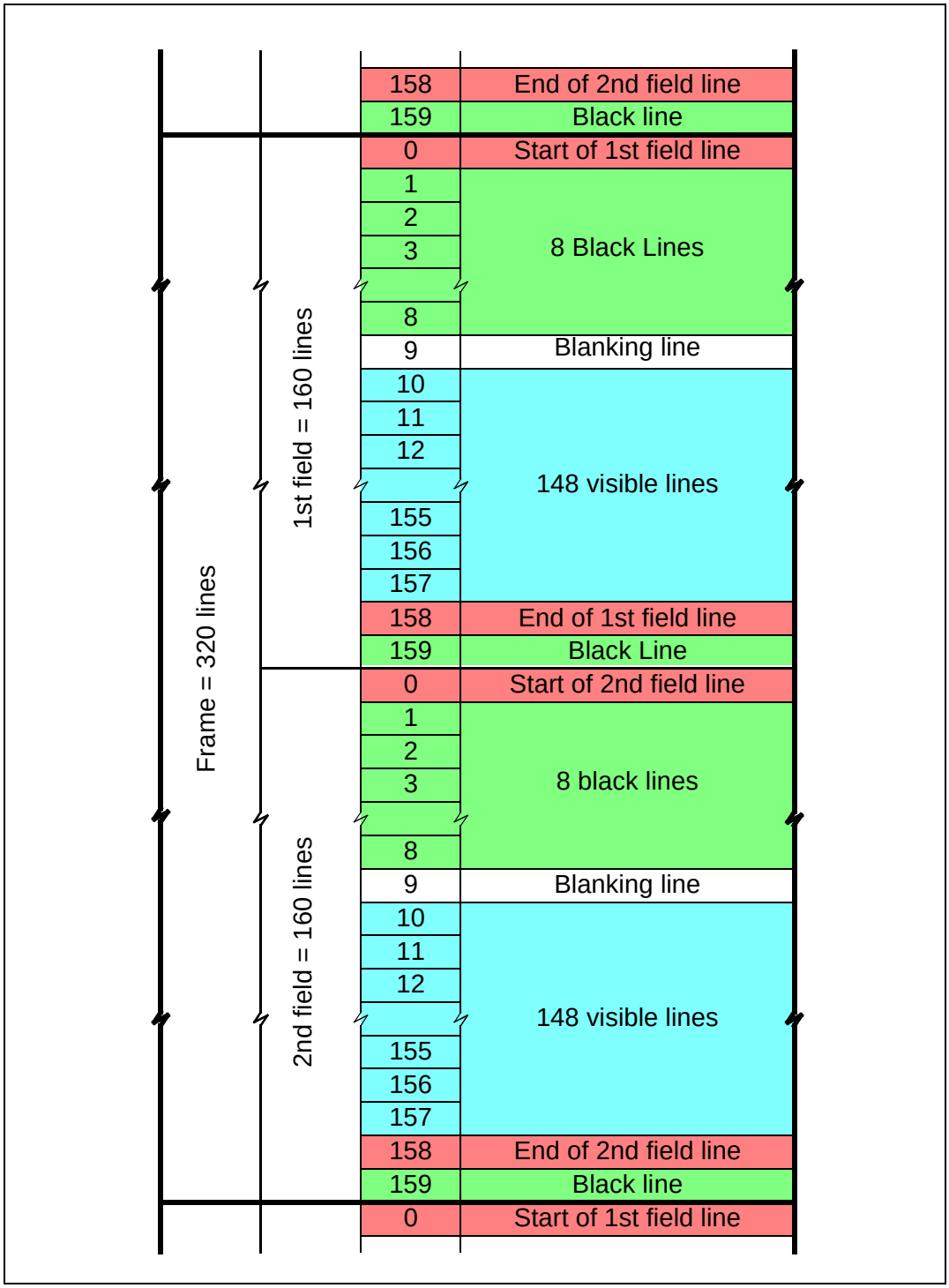
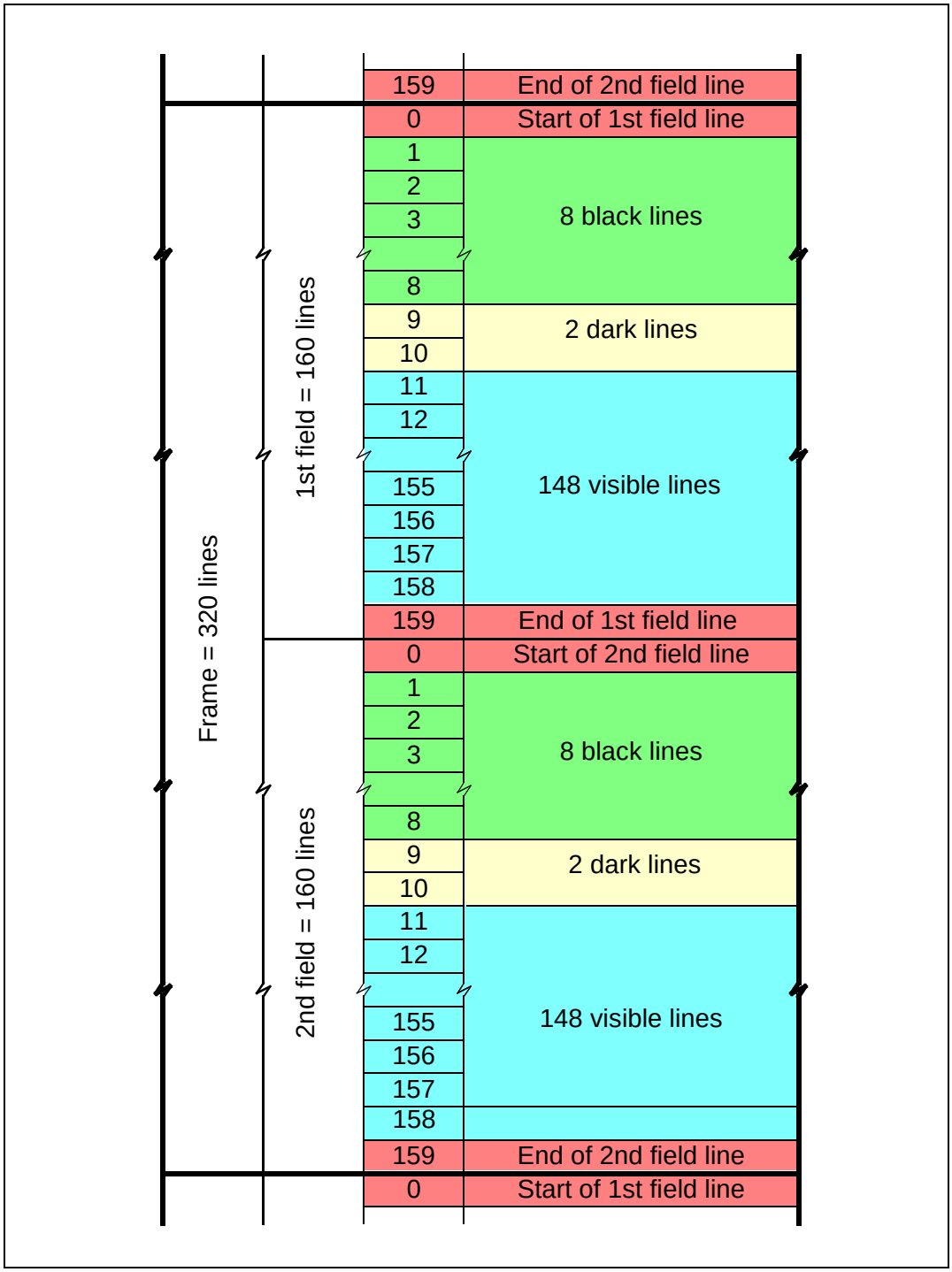


Figure 26: QCIF field and frame formats - VP3 mode off



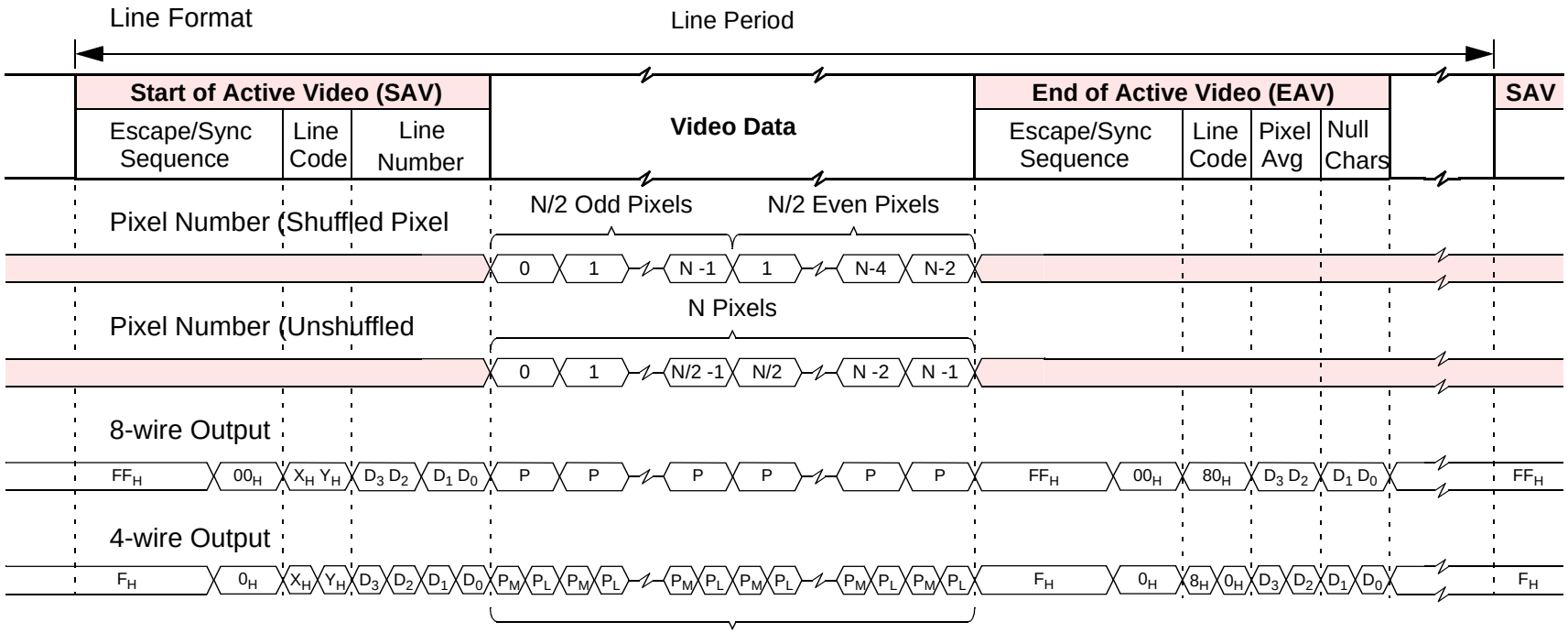
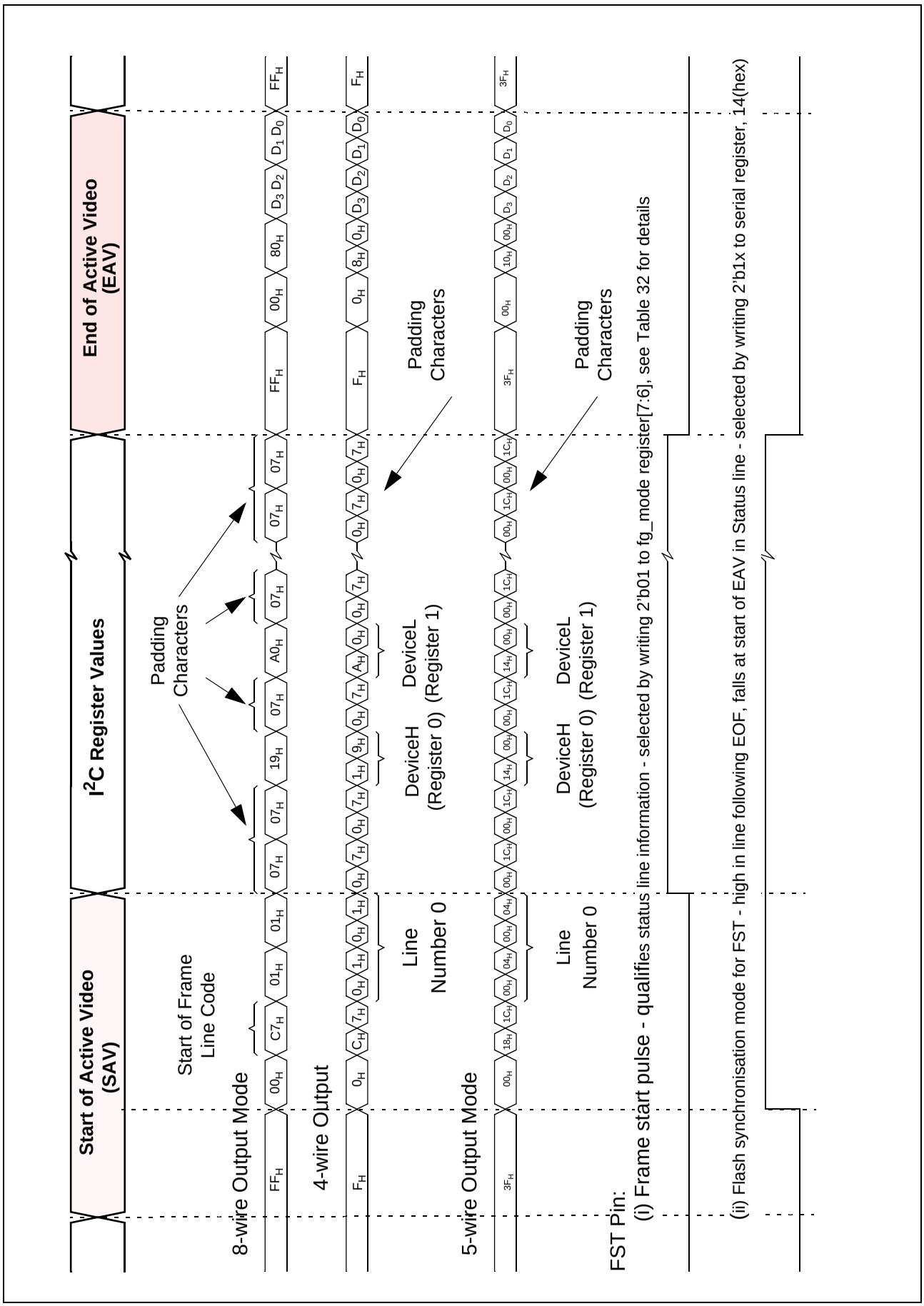


Figure 27: Line data format

(i)	Blanking Line (BL)	P = Blanking Level (07_H)
(ii)	Black Line (BK)	P = Valid Black Pixel Data
(iii)	Visible Line (VL)	P = Valid Pixel Data
(iv)	Start of Frame (SOF)	P = Sensor Status Data, data at pixel position 0 and 1 set to blanking level, 07_H.
(v)	End of Frame (EOF)	P = Blanking Level (07_H)

P_M = Pixel Value - Most Significant Nibble, P_L = Pixel Value - Least Significant Nibble, P = 8-bit Pixel Value

Figure 28: Status line data format and FST signals



7.2.5 Valid video line timing

Active video lines contain valid video data. The pixel data is a continuous stream of bytes within the active lines. Pixel data may be separated from the line header and end-of-line control sequence by a number of 'blank' bytes (07_H).

7.2.6 Start of frame line timing

The start of frame line beginning each video field does not contain video data but the contents of the I^2C register map. Immediately following the SAV sequence, there are 2 padding pixels (see *Figure 27*) output as blanking levels (07_H). There will be more blanking codes output after all the I^2C registers have been output. Padding pixels are output until they are terminated by an end-of-line control sequence. To ensure that no escape/sync characters, (the reserved FF,FF,00 sequence), appear in the sensor status/configuration information, the 07_H code is output after each I^2C value.

If a I^2C register location is unused, a default value corresponding to the DeviceH register is output. The read-out order of the registers is independent of whether the pixel read-out order is shuffled or un-shuffled.

7.2.7 End of frame line timing

The end of frame line contains no video data. Its sole purpose is to indicate the end of a frame.

7.3 Sensor detection using data bus state

At power-up, a sensor pulls all data lines high and these lines remain high while the device is in the power up default, low power state. The device quits this low power mode via the I^2C host write to sensor register setup0 [address 10_{16}]. When the device exits the low power mode, it follows a defined power up sequence (see *Figure 31*). Upon completion of the power up sequence the sensor starts streaming video.

7.4 Sensor resetting via the I^2C

Bit 2 of setup0 register allows the VV5411/VV6411 sensor to be reset to its power-on state via the I^2C. Setting this "Soft Reset" bit causes all the I^2C registers including the "Soft Reset" bit to be reset to their default values. This "Soft Reset" leaves the sensor in low-power mode.

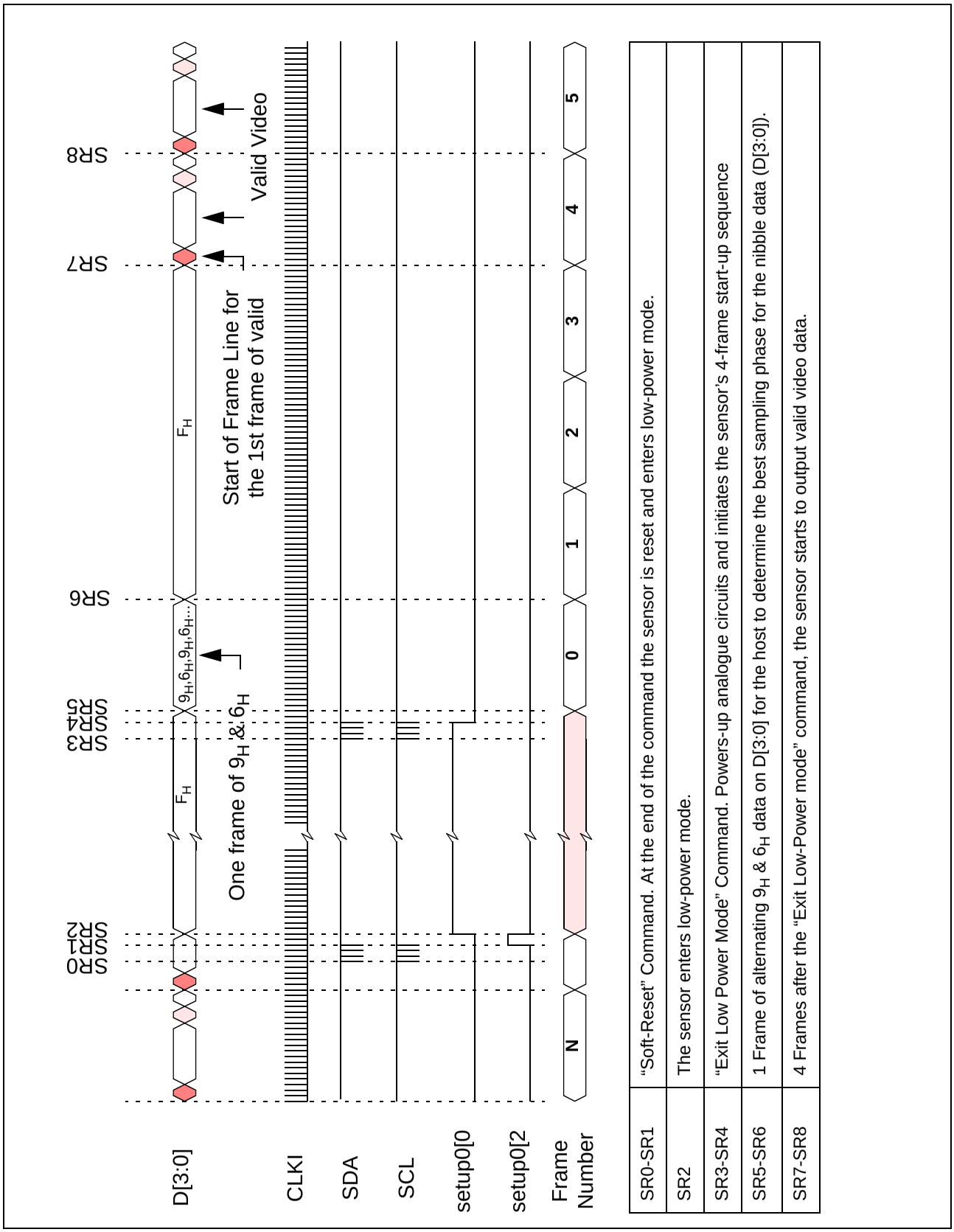
7.5 Sensor resetting via the RESETB pin

At power-up, the RESETB pin is configured as an active low system reset which has the same effect as a soft reset issued via the I^2C as described above.

7.6 Sensor re-synchronizing via the RESETB pin configured as SINB

Bit 5 of the pin mapping register [21] allows the RESETB pin to be re-configured as an active low (edge triggered) system synchronization signal which resets the video timing to the beginning of a field but does NOT reset the serial registers. Therefore, the host does not need to reconfigure the sensor after a re-synchronization.

Figure 29: Sensor resetting via the I²C (example shown is 4wire output mode)



SR0-SR1	"Soft-Reset" Command. At the end of the command the sensor is reset and enters low-power mode.
SR2	The sensor enters low-power mode.
SR3-SR4	"Exit Low Power Mode" Command. Powers-up analogue circuits and initiates the sensor's 4-frame start-up sequence
SR5-SR6	1 Frame of alternating 9_H & 6_H data on D[3:0] for the host to determine the best sampling phase for the nibble data (D[3:0]).
SR7-SR8	4 Frames after the "Exit Low-Power mode" command, the sensor starts to output valid video data.

7.7 Power-up, low-power and sleep modes

Please note that these descriptions of low power and sleep modes assume that the user has selected the optional 4-wire output mode so that D[3:0] transmits the digital video data. When the 5-wire or 8-wire modes are selected, the basic behavior is the same, the contents of the data bus slightly differs.

Table 15: Typical system power-up

PU0	System power up
PU1	Sensor enters low power mode and data bus bits driven high.
PU2	Host enables the sensor clock, CLKI.
PU3-PU4	The host sends a “Soft-Reset” command to the sensor via the I^2C. This ensures that the sensor is in low-power mode.
PU5	Host issues command to remove sensor from low-power mode.
PU6-PU7	Sensors begins execution 4 frame start sequence.
PU8-PU9	One frame of alternating 9_H & 6_H data on D[3:0] for the host to determine the best sampling phase for video data.
PU10-PU11	4 Frames after the “Exit Low-Power Mode” serial comms, the sensor starts to output valid video data.

7.7.1 Power-up/down (*Figure 30*)

The sensor enters low-power mode at power-up. At power-up, all of the data bus lines are immediately driven high and the device is in low-power mode (*Section 7.7.2*).

The sensor remains in low power mode until the external host sends the appropriate message via I^2C to clear the low power bit - bit0 of serial register, setup0, index 10_{16}.

After the “Exit Low-Power Mode” command has been sent, the sensor outputs a continuous stream of alternating 9_H and 6_H values on D[3:0] for one frame. The patterns generated with 5 and 8 wire modes are given in *Table 16* below. By looking at the resulting 0101/1010 patterns appearing on the data bus lines, the host can determine the best sampling position for the nibble data. After the last 9_H 6_H pair has been output, the data bus returns to F_H ($1F_H$ in 5 wire mode) until the fifth frame starts. At this point, the first active video frame is output. Once the host has determined the correct sampling position for the data, it waits for the next start of frame line (SOF).

Figure 30: Typical system power-up procedure

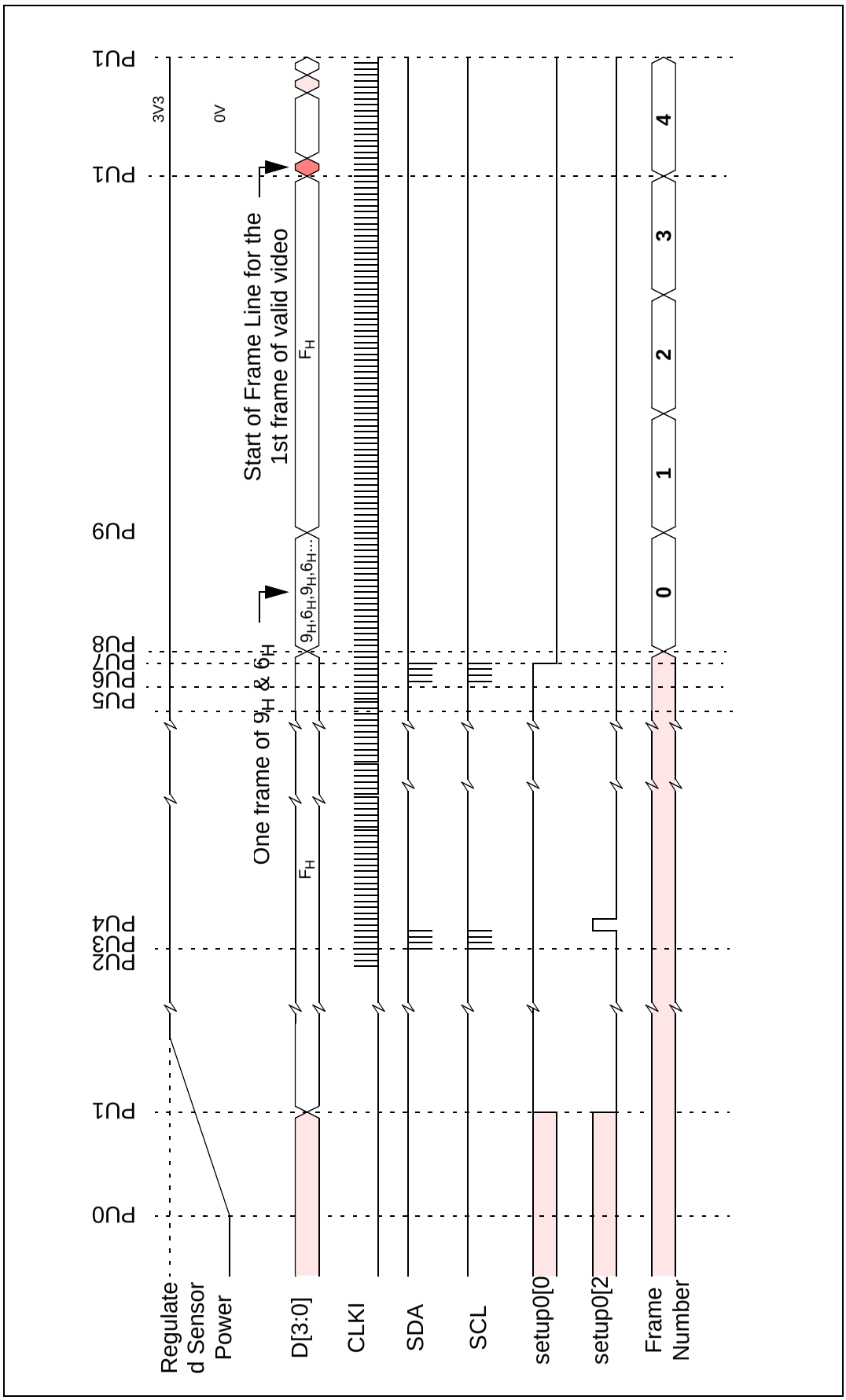


Table 16: Output data bus patterns for determination of best sampling position

Mode	10-bit Value	Output Data Bus Pattern
4-Wire	258_H	$9_H/6_H$ ($1001_2/0110_2$)
5-Wire	136_H	$09_H/16_H$ ($01001_2/10110_2$)
8-Wire	096_H / 069H	$25_H/1A_H$ ($00100101_2/00011010_2$)

7.7.2 Low-power mode (*Figure 31*)

The sensor analog circuitry is powered down and then powered on via I^2C control. When the low-power bit is set via the I^2C, all the data bus lines go high at the end of frame line of the current frame. At this point, the analog circuits in the sensor are powered down. The system clock must remain active for the duration of low power mode.

During low power mode, only the analog circuits are powered down while the values of the I^2C registers e.g. exposure and gain are preserved. The internal frame timing is reset at the start of a video frame on exiting low-power mode. In a similar manner as in the previous section, the first frame following the serial comms contains a continuous stream of alternating 9_H and 6_H - or equivalent for the alternative output databus widths - to allow the host to re-confirm its sampling position. Three frames later, the first start of frame line is generated.

7.7.3 Sleep mode

Sleep mode is similar to low-power mode except that analog circuitry remains powered. When the sleep command is received via the I^2C, the pixel array is reset and all the data lines go high at the end of the current frame. Again the system clock must remain active for the duration of sleep mode.

When sleep mode is disabled, the CMOS sensor’s frame timing is reset at the start of a frame. During the first frame following the exit from sleep mode, the data bus remains high while the exposure value propagates through the pixel array. At the start of the second frame, the first start of field line is generated.

7.7.4 System clock status during sensor low-power modes

The sensor enters and exits the low power and sleep modes only if the system clock, CLKI, is active.

7.8 Suspend mode

Under the control of the SUSPEND pin, VV5411/VV6411 can be forced into an ultra low power mode. The sensor current consumption is less than 80µA while suspended. While the sensor is in this mode, video output is turned off and no serial communications can occur.

The SUSPEND mode is effectively identical to a power on reset - all the video timing blocks within the sensor are reset as well as the I^2C contents. Therefore, the user will have to perform a complete reconfiguration of the device when exiting SUSPEND. The sensor will also repeat the full 4 field power up sequence.

Table 17: VV5411/VV6411 suspend mode power consumption

Mode	Description	Sensor current (approx.)
Suspend	Sensor in lowest power state. Suspend has been asserted by host.	c.80µA

7.9 Data qualification clock, QCK

VV5411/VV6411 provides a data qualification clock (see *Figure 32*) to qualify the information output on data bus. The sensor can generate two types of qualification clock:

- Fast QCK clock at nibble rate. The falling edge of this clock qualifies data.
- Slow QCK clock at pixel rate. Both the falling and rising edge of this clock are used to qualify data. The most significant data nibble is qualified by the rising edge of the slow QCK and the least significant nibble is qualified by the falling edge of the slow QCK.

There are 4 modes of QCK operation:

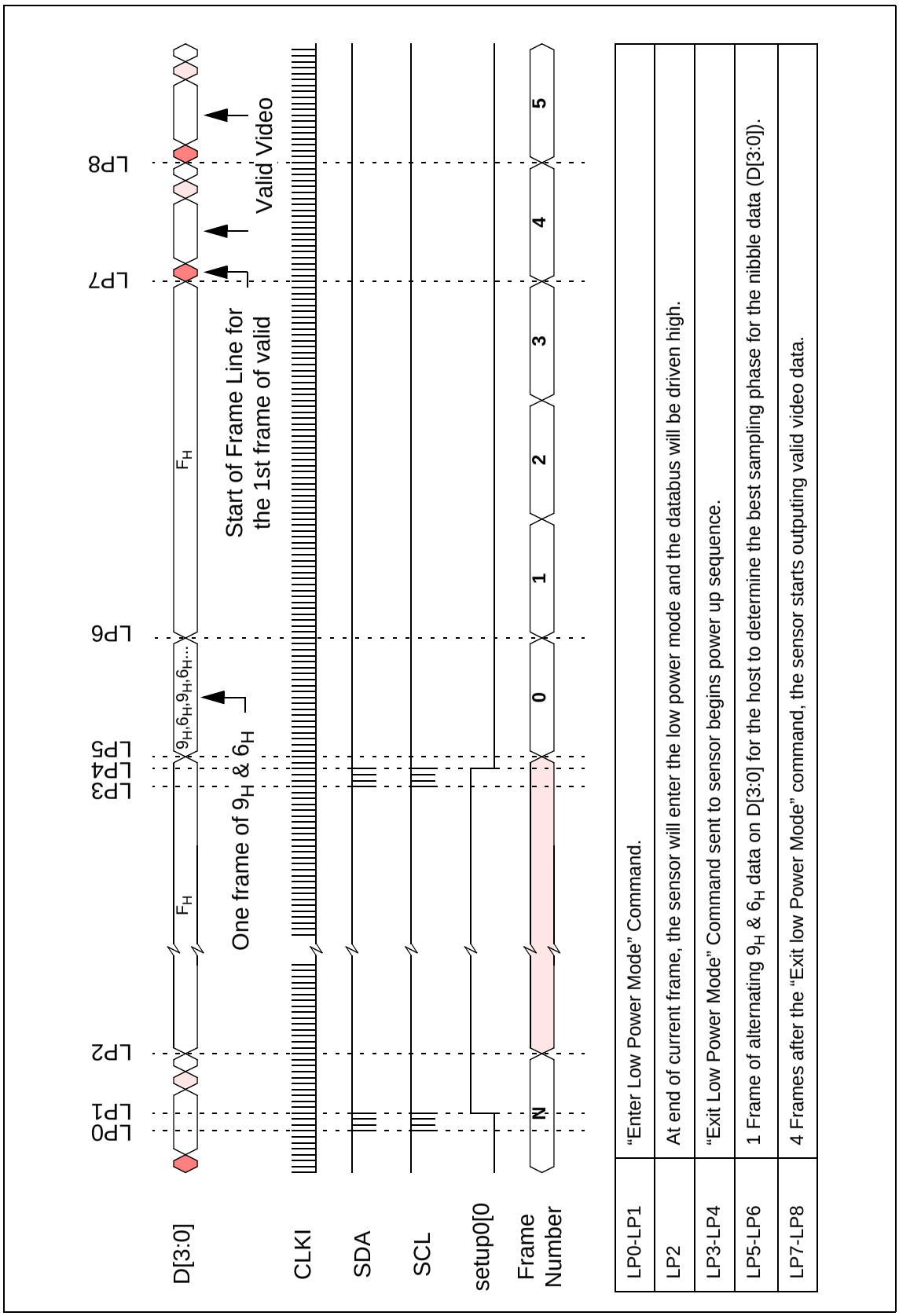
- disabled (always low - default mode of operation)
- free running - qualifies the entire output data stream
- qualify embedded control sequences, status data, (from the SOF line), and pixel data
- qualify pixel data only (this will include data from the black lines).

The operating mode for QCK is set via the I^2C. The QCK output can be tri-stated either when OEB is driven high or via the appropriate control bit in the I^2C (see data_format register[22]).

The QCK pin can also be configured to output the state of a I^2C register bit. This feature allows the sensor to control external devices, e.g. stepper motors, shutter mechanisms.

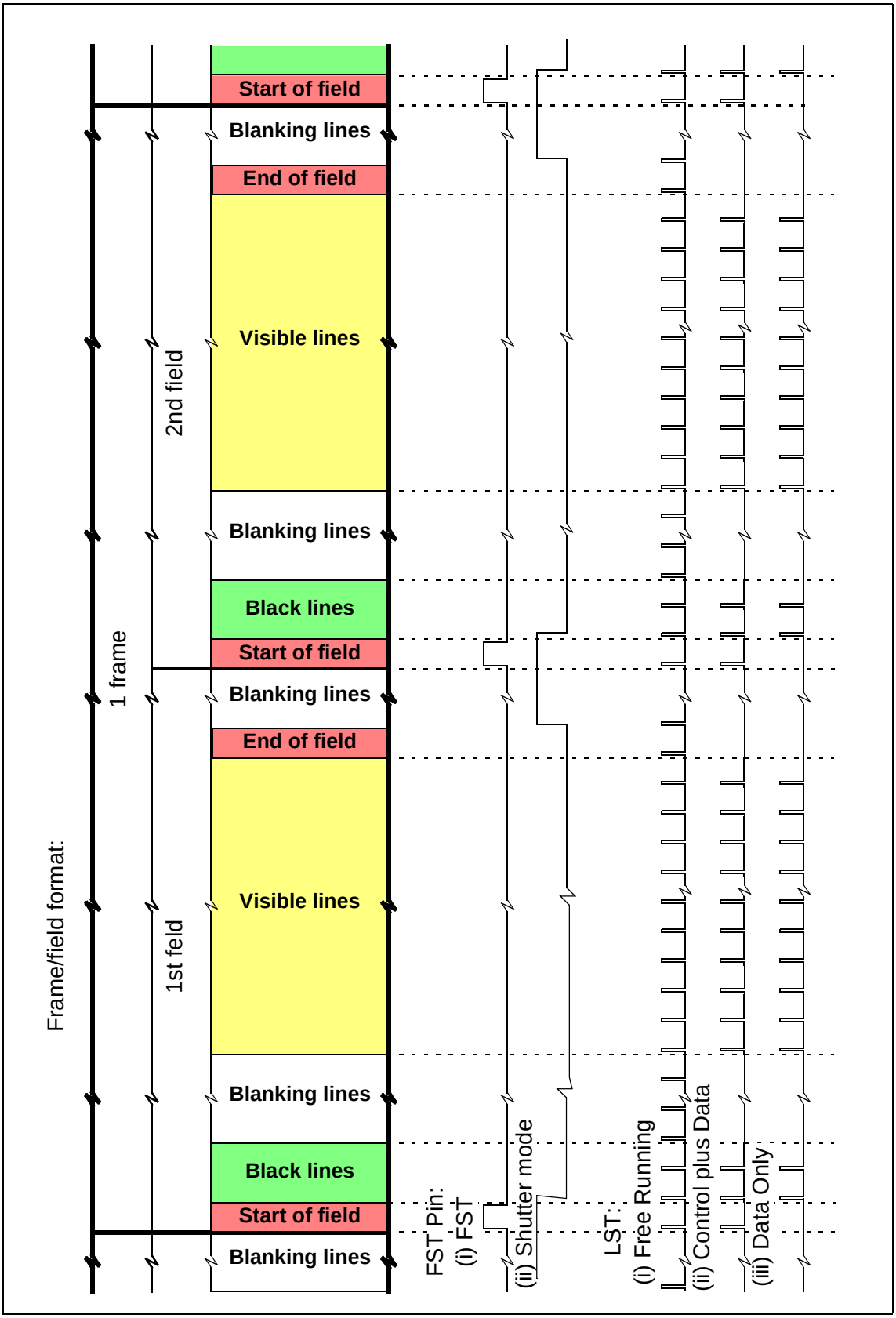
Full details of how to configure the QCK output pin are given in in 2 registers fg_mode[20] and pin_mapping[21].

Figure 31: Entering and exiting low power mode (example is 4wire mode).



LP0-LP1	"Enter Low Power Mode" Command.
LP2	At end of current frame, the sensor will enter the low power mode and the databus will be driven high.
LP3-LP4	"Exit Low Power Mode" Command sent to sensor begins power up sequence.
LP5-LP6	1 Frame of alternating 9_H & 6_H data on D[3:0] for the host to determine the best sampling phase for the nibble data (D[3:0]).
LP7-LP8	4 Frames after the "Exit low Power Mode" command, the sensor starts outputing valid video data.

Figure 32: Frame/field level timings for FST and LST



7.9.1 Line Start Signal, LST

There are 4 modes of operation for the LST pin programmable via the I^2C (see fg_mode[20]):

- disabled (always low- default)
- free running - LST signal occurs once at the beginning of every line.
- All lines except blanking lines are qualified by LST.
- Only Black and Visible Lines are qualified by LST.

The LST is tri-stated either when OEB is driven high or via the appropriate control bit in the I^2C, (see data_format register[22]). *Table 18* below details the LST timing for the different video modes, (see *Figure 33* for specification of t1 and t2).

Table 18: LST timing

Video mode	t1		t2	
	pck's	us	pck's	us
CIF	21	5.25	16	4.000
QCIF (both pan tilt and subsampled, 16MHz clock)	6	6.00	15	15.00
QCIF (both pan tilt and subsampled, 8MHz clock)	6	6.00	15	15.00
PAL	33	4.652	42	5.962
NTSC	27	4.714	12	2.095

7.9.2 Frame Start Signal, FST

There are 3 modes of operation for the FST pin programmable via the I^2C:

- disabled (always low- default)
- frame start signal (FST). The FST signal occurs once in every frame, is high for 356 pixel periods (712 system clock periods) and qualifies the data in the start of frame line.
- Shutter/electronic flash synchronization signal - FST rises a the start of the video data in the first black/blank line after the EOF line and falls at the end of data in the SOF line.

The FST output is tri-stated either when OEB is driven high or via the appropriate control bit in the I^2C, (see data_format register[22]).

The configuration details for FST are given fg_mode register[20].

Figure 33: Line level timings for FST and LST

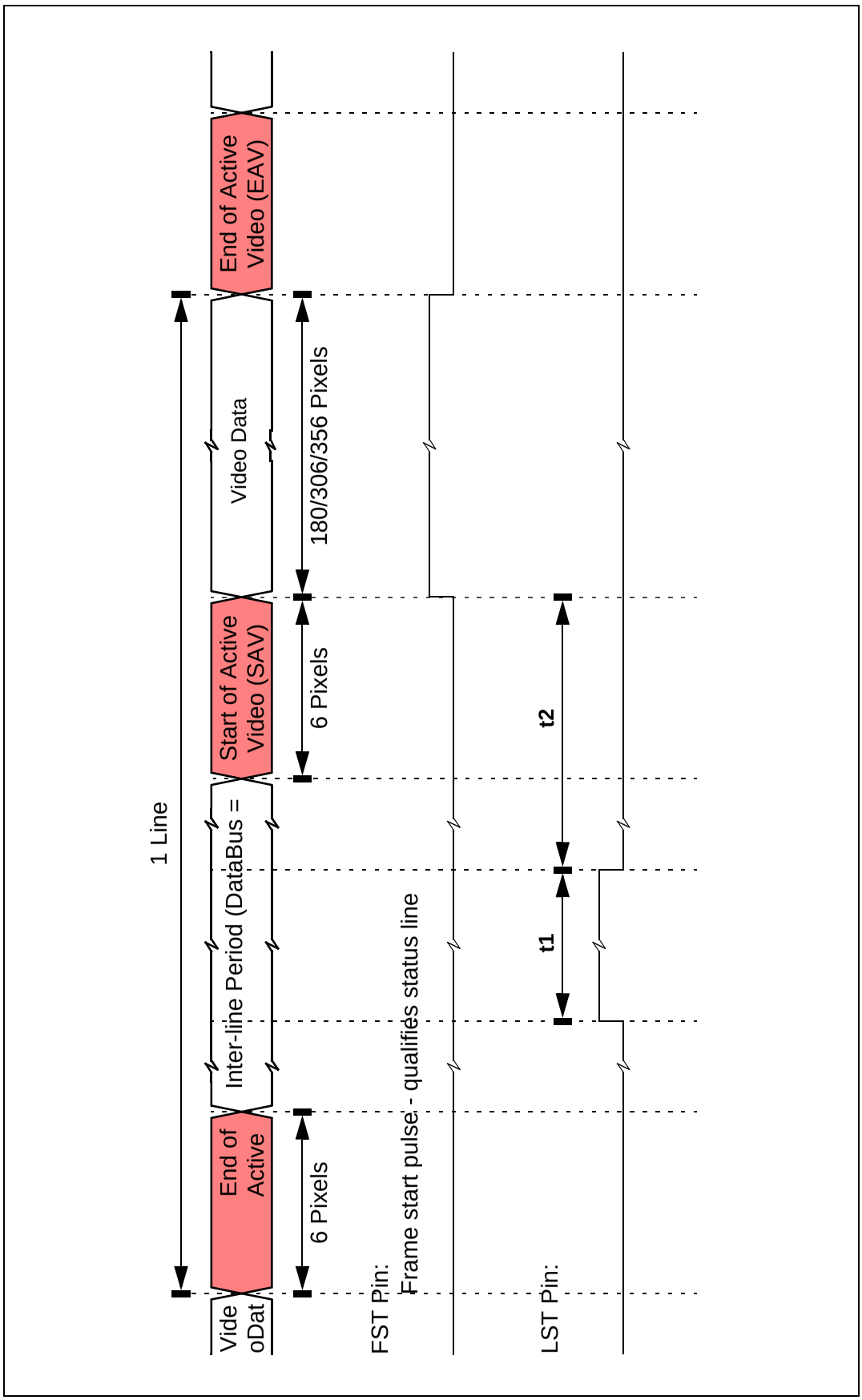
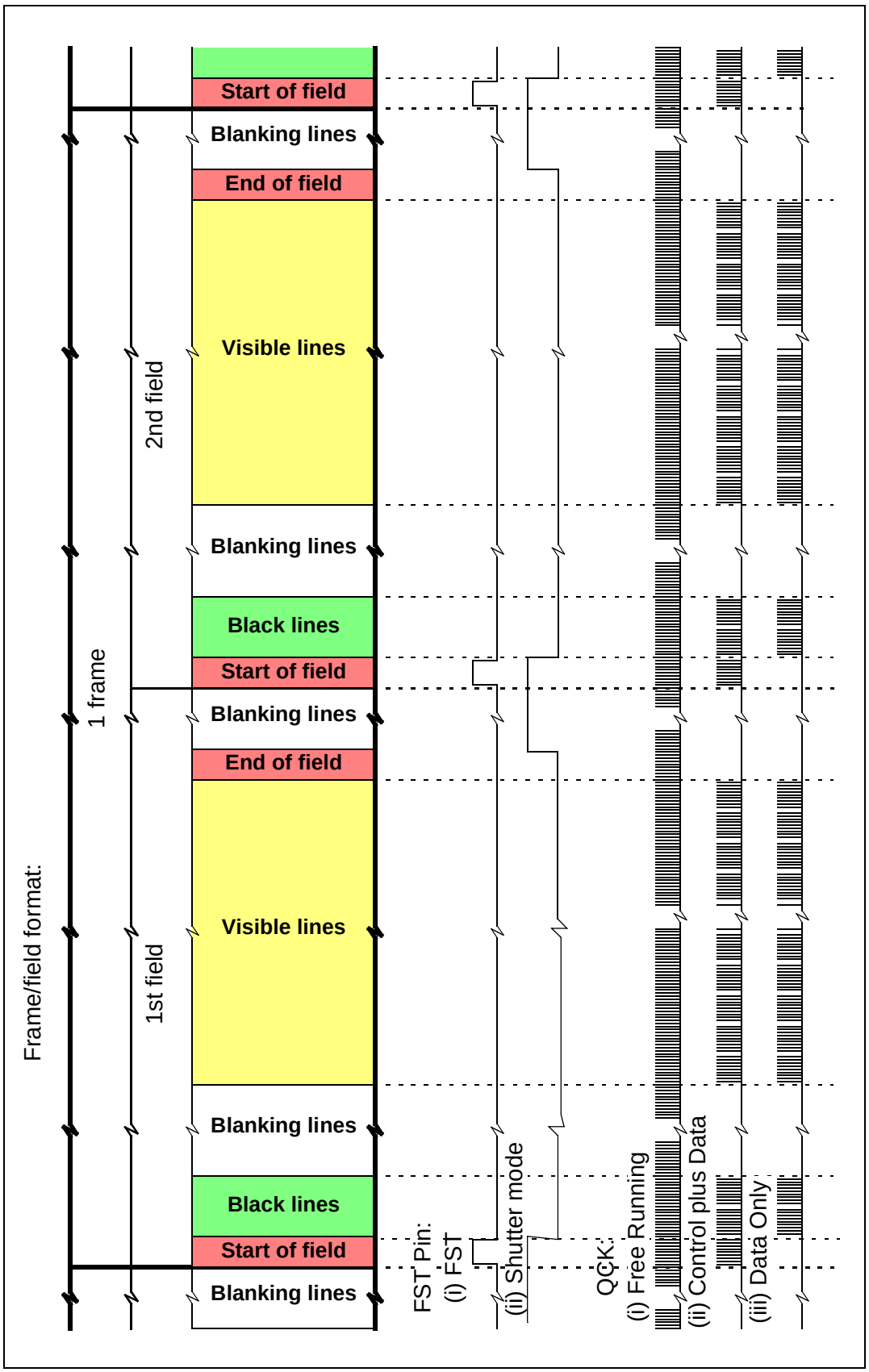


Figure 34: Frame/field level timings for FST and QCK



8 Serial Control Bus

8.1 General description

The writing of configuration information to the video sensor and the reading of both sensor status and configuration information back from the sensor are performed via the 2-wire I^2C.

Communication using the serial bus centres around a number of registers internal to the video sensor. These registers store sensor status, set-up, exposure and system information. Most of the registers are read/write allowing the receiving equipment to change their contents. Others (such as the chip id) are read only.

The main features of the I^2C include:

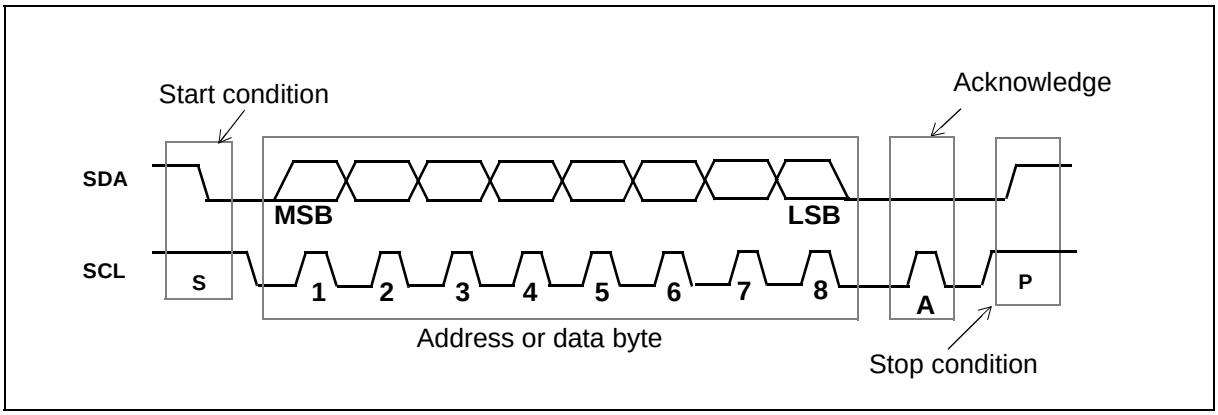
- Variable length read/write messages.
- Indexed addressing of information source or destination within the sensor.
- Automatic update of the index after a read or write message.
- Message abort with negative acknowledge from the master.
- Byte oriented messages.

The contents of all internal registers accessible via the serial control bus are encapsulated in each start-of-field line - see *Section 7.2.6*.

8.2 Serial communication protocol

The co- processor or host must perform the role of a communications master while the camera acts as a slave receiver or a transmitter.The communication from host to camera is an 8-bit data with a maximum serial clock host frequency of up to 100 kHz. Since the serial clock is generated by the bus master, it determines the data transfer rate. Data transfer protocol on the bus is illustrated in *Figure 35*.

Figure 35: I^2C data transfer protocol



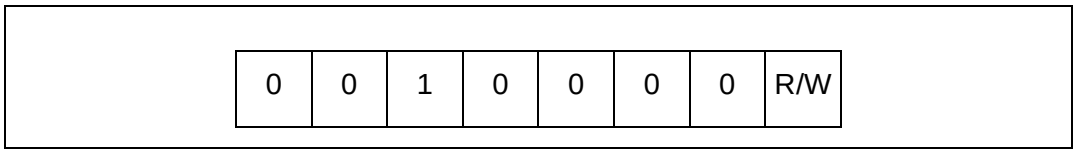
8.2.1 Data format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is produced by sampling *sda* at a rising edge of *scl*. The external data must be stable during the high period of *scl*. Exceptions are *start* (S) or *stop* (P) conditions when *sda* falls or rises respectively, while *scl* is high.

A message contains at least two bytes preceded by a *start* condition and followed by either a *stop* or *repeated start, (Sr)* followed by another message.

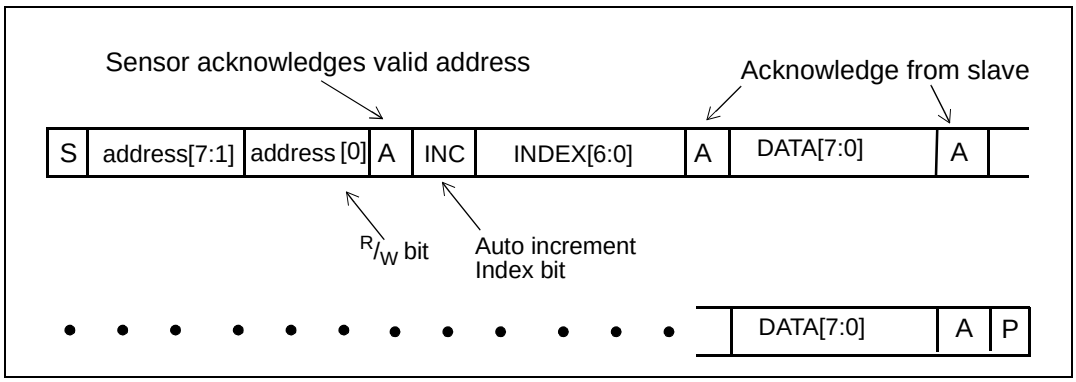
The first byte contains the device address byte which includes the data direction *read* (r)*, ~write*, (~w) bit. The lsb of the address byte indicates the direction of the message. If the lsb is set high, the master reads data from the slave and if the lsb is reset low, the master writes data to the slave. After the *r, ~w* bit is sampled, the data direction cannot be changed until the next address byte with a new *r, ~w* bit is received.

Figure 36: VV5411/VV6411 I²C address



The byte following the address byte contains the address of the first data byte (also referred to as the *index*). The I^2C can address up to 128-byte registers. If the msb of the second byte is set, the automatic increment feature of the address index is selected.

Figure 37: I^2C Data format



8.2.2 Message interpretation

All I^2C communications with the sensor must begin with a *start* condition. If the *start* condition is followed by a valid address byte then further communications can take place. The sensor will acknowledge the receipt of a valid address by driving the *sda* wire low. The state of the *read/~write* bit (lsb of the address byte) is stored and the next byte of data, sampled from *sda,* can be interpreted.

During a write sequence, the second byte received is an address index used to point to one of the internal registers. The msbit of the following byte is the *index auto increment* flag. If this flag is set then the I^2C automatically increments the index address by one location after each slave acknowledge. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a *stop* condition or sends a *repeated start*, *(Sr)*. If the auto increment feature is used, the master does *not* have to send indexes to accompany the data bytes.

As data is received by the slave, it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the current index is read out in the byte following the device address byte. The next byte read from the slave device are the contents of the register addressed by the current

index. The contents of this register are then parallel loaded into the serial/parallel register and clocked out of the device by *scl.*

At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. Although VV5411/VV6411 is always considered to be a slave device, it acts as a transmitter when the bus master requests a read from the sensor.

At the end of a sequence of incremental reads or writes, the terminal index value in the register will be one *greater* than the last location read from or written to. A subsequent read will use this index to begin retrieving data from the internal registers.

A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge after reading a complete byte during a read operation.

8.2.3 The programmers model

There may be up to 128, 8-bit registers within the camera, accessible by the user via the I^2C. They are grouped according to functions with each group occupying a 16-byte page of the location address space. There may be up to eight of such groups, although this scheme is purely a conceptual feature, not related to the actual hardware implementation. The primary categories are given below:

- Status registers (Read only).
- Setup registers with bit significant functions.
- Exposure parameters that influence output image brightness.
- System functions and analog test bit significant registers.

Any internal register that can be written to can also be read from. There are a number of read only registers that contain device status information, (e.g. design revision details).

Names that end with H or L denote the most or least significant part of the internal register. Note that unused locations in the H byte are packed with zeroes.

STMicroelectronics sensors that include a 2-wire I^2C are designed with a common address space. If a register parameter is unused in a design, but has been allocated an address in the generic design model, the location is referred to as ***reserved***. If the user attempts to read from any of these ***reserved or unused*** locations, a default byte will be read back. In the VV5411/VV6411, this data is 19_H. A write instruction to a reserved (but unused) location is illegal and will not be successful as the device will not allocate an internal register to the data word contained in the instruction.

A detailed description of each register follows. The address indexes are shown as decimal numbers in brackets [....] and are expressed in decimal and *hexadecimal* respectively.

Table 19 : I²C address map.

$Index_{10}$	$Index_{16}$	Name	Length	R/W	Default	Comments
Status Registers - [0-15]						
0	0	deviceH	8	RO	0001_1001_2	Chip identification number including revision indicator
1	1	deviceL	8	RO	1010_0000_2	
2	2	status0	8	RO	0001_0000_2	User can determine whether timed I²C data has been consumed by interrogating flag states
3	3	line_countH	8	RO	n/a	Current line counter value
4	4	line_countL	8	RO	n/a	
5	5	xendH	1	RO	359	End x coordinate of image size
6	6	xendL	8	RO		
7	7	yendH	1	RO	293	End y coordinate of image size
8	8	yendL	8	RO		
9	9	dark_avgH	4	RO	0	This is the average pixel value returned from the dark line offset cancellation algorithm (2's complement notation)
10	A	dark_avgL	8	RO	0	
11	B	black_avgH	4	RO	0	This is the average pixel value returned from the black line offset cancellation algorithm (2's complement notation)
12	C	black_avgL	8	RO	0	
13	D	status1	2	RO	00	Flags to indicate whether the x or y image coordinates have been clipped
14-15	E-F	unused				
Setup Registers - [16-31]						
16	10	setup0	8	R/W	0000_1001_2	Low-power/sleep modes & video timing
17	11	setup1	8	R/W	1100_0000_2	Various parameters
18	12	sync_value	8	R/W	0001_1111_2	Contains pixel counter reset value used by external sync
19	13	reserved				
20	14	fg_modes	8	R/W	0000_0000_2	Frame grabbing modes (FST, LST and QCK)
21	15	pin_mapping	7	R/W	000_1000_2	FST and QCK mapping modes.
22	16	data_format	8	R/W	0000_0001_2	Data resolution
23	17	op_format	7	R/W	001_1000_2	Output coding formats
24	18	mode_select	2	R/W	01_2	Various mode select bits
25 - 31	19-1F	unused				

Table 19 : I²C address map.

$Index_{10}$	$Index_{16}$	Name	Length	R/W	Default	Comments
Exposure Registers - [32-47]						
32	20	fineH	2	R/W	0	Fine exposure.
33	21	fineL	8	R/W		
34	22	coarseH	2	R/W	302	Coarse exposure
35	23	coarseL	8	R/W		
36	24	analog gain	8	R/W	1111_0000	Analog gain setting
37	25	clk_div	4	R/W	0	Clock division
38-43	26-2B	reserved				
44	2C	dark offsetH	3	R/W	0	dark line offset cancellation value (2's complement notation)
45	2D	dark offsetL	8	R/W		
46	2E	dark offset setup	7	R/W	$0110\ 0001_2$	dark line offset cancellation enable
47	2F	reserved				
Color Registers - [48-79]						
48 - 79	30-4F	reserved	8	R/W		
Video Timing Registers - [80-103]						
80-81	50-51	reserved				
82	52	line_lengthH	2	R/W	415	Line length (pixel clocks)
83	53	line_lengthL	8	R/W		
84 - 86	54-56	reserved				
87	57	x-offsetH	1	R/W	5	x-co-ordinate of top left corner of region of interest (x-offset)
88	58	x-offsetL	8	R/W		
89	59	y-offsetH	1	R/W	3	y-co-ordinate of top left corner of region of interest (y-offset)
90	5A	y-offsetL	8	R/W		
91 - 96	5B-60	reserved				
97	61	field_lengthH	2	R/W	319	Field length (lines)
98	62	field_lengthL	8	R/W		
99-102	63-66	reserved				
103	67	unused		R/W		
Text Overlay Registers - [104-107]						
104 - 105	68-69	reserved				
106 - 107	6A-6B	unused				
I²C Autoload Registers - [108-111]						
108 - 109	6C-6D	reserved				
110 - 111	6E-6F	unused				

Table 19 : I²C address map.

$Index_{10}$	$Index_{16}$	Name	Length	R/W	Default	Comments
System Registers - [112-127]						
112	70	black offsetH	3	R/W	- 64	black offset cancellation default value (2's complement notation)
113	71	black offsetL	8	R/W		
114	72	black offset setup	6	R/W	$0011\ 0001_2$	black offset cancellation setup
115	73	unused				
116	74	reserved				
117	75	cr0	8	R/W	$0000\ 0000_2$	Analog control register 0
118	76	cr1	8	R/W	$0000\ 0000_2$	Analog control register 1
119	77	as0	8	R/W	$0101\ 1010_2$	ADC setup register
120	78	at0	8	R/W	$0000\ 0000_2$	Analog test register
121	79	at1	8	R/W	$0000\ 0001_2$	Audio amplifier setup register
122 - 125	7A-7D	unused				
126	7E	reserved				
127	7F	reserved				

8.2.4 Status registers - [0 - 15],*[0-F]*

[0-1],*[0-1]* - DeviceH and DeviceL

These registers provide read only information that identifies the sensor type having been coded as a 12-bit number and a 4-bit mask set revision identifier. The device identification number for VV5411/VV6411 is 411 i.e. $0001\ 1001\ 1010_2$. The initial mask revision identifier is 0 i.e. 0000_2.

Table 20: [0],*[0]* - DeviceH

Bits	Function	Default	Comment
[7:0]	Device type identifier	$0001\ 1001_2$	Most significant 8 bits of the 12 bit code identifying the chip type.

Table 21: [1],*[1]* - DeviceL

Bits	Function	Default	Comment
[7:4]	Device type identifier	1010_2	Least significant 4 bits of the 12 bit code identifying the chip type.
[3:0]	Mask set revision identifier	0000_2	

[2],*[2]* - Status0

Table 22 : [2],*[2]* - Status0

Bit	Function	Default	Comment
0	Fine exposure value update pending	0	Fine exposure value sent but not yet consumed by the sensor
1	Coarse exposure value update pending	0	Coarse exposure value sent but not yet consumed by the sensor
2	Gain value update pending	0	Gain value sent but not yet consumed by the sensor
3	Clock division update pending	0	Clock divisor sent but not yet consumed by the sensor
4	Odd/even frame	1	The flag will toggle state on alternate frames
5	Pan image parameters pending	0	Pan image parameters sent but not yet consumed by the sensor
6	Tilt image parameters pending	0	Tilt image parameters sent but not yet consumed by the sensor
7	Video timing parameter update pending flag	0	Video timing parameters sent but not yet consumed by sensor

[3-4],*[3-4]* - Line_countH & Line_countL

Table 23: [3-4],*[3-4]* - Current line counter value

Register index	Bits	Function	Default	Comment
3	0	Current line count MSB	-	Displays current line count
4	[7:0]	Current line count LSB	-	

[5-6],*[5-6]* - XendH & XendL

Table 24: [5-6],*[5-6]* - Xend

Register index	Bits	Function	Default	Comment
5	0	Xend msb's	359	These registers contain the end x coordinate of the read out image size, (the x offset register contains the start x coordinate)
6	[7:0]	Xend ls byte		

[7-8],*[7-8]* - YendH & YendL

Table 25: [7-8],*[7-8]* - Yend

Register index	Bits	Function	Default	Comment
5	0	Yend ms bits	293	These registers contain the end y coordinate of the read out image size, (the y offset register contains the start y coordinate)
6	7:0	Yend ls byte		

[9-12],*[9-C]* - Black_Avg & Dark_Avg

Table 26 : [9-12],*[9-C]* - Black & Dark Averages

Register index	Bits	Function	Default	Comment
9	[3:0]	Dark avg ms bits	0	The calculated pixel average over a series of dark lines (1,2 or 4 lines). The pixel sample size from each dark line will be image size dependent up to a maximum of 256. The average value is a signed 12 bit number
10	[7:0]	Dark avg ls byte	0	
11	[3:0]	Black avg ms bits	0	The calculated pixel average over a series of black lines (4 or 8 lines). The pixel sample size from each black line will be image size dependent up to a maximum of 256. The average value is a signed 12-bit number
12	[7:0]	Black avg ls byte	0	

[13],*[D]* - Status1 register

Table 27: [13],*[D]* - Status1

Bit	Function	Default	Comment
0	X image parameters clipped	0	If this bit is set, the current x offset parameter requested has caused the x coordinates to be clipped
1	Y image parameters clipped	0	If this bit is set, the current y offset parameter requested has caused the y coordinates to be clipped
[7:2]	unused	000000	

[14-15],*[E-F]* - unused

8.2.5 Setup registers - [16 - 31],*[10-1F]*

[16],*[10]* - Setup0[

Table 28: [16],*[10]* - Setup0

Bit	Function	Default	Comment
0	Low power mode: Off / **On**	1	Powers down the sensor array. The output data bus goes to F_H. At power-up the sensor enters low power mode.
1	Sleep mode: **Off** / On	0	Puts the sensor array into reset. The output data bus goes to F_H.
2	Soft reset **Off** / On	0	Setting this bit resets the sensor to its power-up defaults. This bit is also reset.
3	Frame/field rate select: 25 fps (PAL) / **30 fps (NTSC)**	1	
[5:4]	Reserved	00	
[7:6]	Video timing mode select	00	00 - CIF timing modes 01 - PAL/NTSC 3.2 fsc timing modes 10 - pan/tilt/QCIF timing modes If this mode is selected a QCIF size image is output. The coordinates which define the top left corner of the QCIF portion of the array to be output are defined by the parameters in registers 88 - 91 inclusive. By default , the x- and y-sizes of the output image are180 & 148 respectively. 11 - sub-sampled QCIF timing modes If this mode is selected a QCIF size image will be output. The CIF image is sub-sampled in groups of 4 to preserve the Bayer pattern with every second group of pixels & lines skipped.

Table 29: Video timing modes

Video mode	setup0 [7:6]	setup0 [3]	System clock divisor	Video data	Line length	Field length	Data format (default)	Comment
1	00	0	4	356 x 292	500	320	5-wire	CIF 25fps
2		1	4	356 x 292	416	320	5-wire	CIF 30fps
3	01	0	2	356 x 292	454	312/313	5-wire	PAL (3.2 fsc)
4		1	2	306 x 244	364	262/263	5-wire	NTSC (3.2 fsc)
5	10	0	8	180 x 148	250	160	5-wire	pan/tilt QCIF 25fps
6		1	8	180 x 148	208	160	5-wire	pan/tilt QCIF 30fps
7	11	0	8	180 x 148	250	160	5-wire	sub-sampled QCIF 25fps
8		1	8	180 x 148	208	160	5-wire	sub-sampled QCIF 30fps

[17],*[11]* - Setup1

Table 30 : [17],*[11]* - Setup1

Bit	Function	Default	Comment
[2:0]	Reserved	000	
3	Enable immediate clock division update. **Off**/On	0	Allow manual change to clock division to be applied immediately
4	Enable immediate gain update. **Off**/On	0	Allow manual change to gain to be applied immediately
5	Enable additional black lines (lines 3-8) **Off**/On	0	If enabled, this bit also enables the lines immediately following the end of frame line. This bit can only set/reset if the VP3 mode (ON) has been selected. In VP3 mode (OFF) operation, all possible black lines are always output.
6	reserved	1	
7	Pixel read-out order (hshuffle) Unshuffled or **Shuffled**	1	If the pixel read out is shuffled, the pixels are read out in colour “blocks”, i.e. all the red pixels followed by all the green pixels and on the following line all the green pixels followed by all the blue pixels and so on. If the unshuffled read out is selected, the pixels are read out in the “normal” interleaved manner that preserved the Bayer pattern.

[18],*[12]* - sync_reset

Table 31 : [18],*[12]* - sync_reset

Bit	Function	Default	Comment
[7:0]	Pixel counter reset value	31	During synchronization, the pixel counter can be reset to the known value or offset by up to 255 pck’s into the pixel count sequence.

[19],*[13]* - reserved

[20],*[14]* - fg_modes

Bits [3:2] of the fg_mode register are mode dependent. If the NTSC or PAL video modes are selected, the free running QCK mode is selected. The slow QCK is selected by default, regardless of the video mode..

Table 32: [20],*[14]* - fg_modes

Bit	Function	Default	Comment
[1:0]	FST/QCK pin modes	00	Selection of FST, QCK pin data
[3:2]	QCK modes	00	00 - if CIF & QCIF mode selected 01 - if NTSC and PAL mode selected
[5:4]	LST modes	00	See Table 35 below for details
[7:6]	FST modes	00	See Table 36 below for details

Table 33: FST/QCK pin selection

fg_mode[1:0]		FST pin	QCK pin
0	0	FST	Slow QCK
0	1	FST	Fast QCK
1	0	Fast QCK	Slow QCK
1	1	Invert of Fast QCK[a]	Fast QCK

a. The FST pin will always output the free running version of QCK (either inverted or normal)

Table 34: QCK modes

fg_mode[3:2]		QCK state
0	0	Off
0	1	Free Running
1	0	Valid during data and control period of line
1	1	Valid only during data period of line

Table 35 : LST modes

fg_mode[5:4]		LST pin
0	0	Off
0	1	Free Running
1	0	Output for black, video data and status lines
1	1	Output only for black and video data lines.

Table 36: FST modes

fg_mode[7:6]		FST pin
0	0	Off
0	1	Normal behavior, FST will qualify the visible pixels in the status line
1	x	Special digital stills mode. FST will be asserted at the beginning of valid data on the line following the EOF line. FST will be cleared at the end of the visible pixels in the following status line.

[21],*[15]* - pin_mapping

Table 37: [21],*[15]* - pin_mapping

Bit	Function	Default	Comment
0	Map I^2C register bits values on to the QCK and FST pins **Off**/On	0	
1	I^2C Bit for QCK pin	0	
2	I^2C Bit for FST pin	0	
[4:3]	Output driver strength select	00	Default setting selects 2mA driver
5	Enable RESETB pin as SIN **Off** / On	0	At power up, the RESETB pin is configured as an active low system reset which synchronizes the video timing logic and resets all serial registers to their default state. Setting this bit configures the RESETB pin as an active high system synchronization signal (SIN) which will synchronize the video timing but will NOT reset the serial registers.
7:6	Unused	0	

Table 38 : FST/QCK pin selection

Mapping Enable	FST pin	QCK pin
0	FST	QCK
1	pin_mapping[2]	pin_mapping[1]

Table 39 : Output driver strength selection

oeb_composite	pin_map[4]	pin_map[3]	Comments
0	0	0	Drive strength = 2mA (Default)
0	0	1	Drive strength = 4mA
0	1	0	Drive strength = 6mA
0	1	1	unallocated
1	x	x	Outputs are not being driven therefore driver strength is irrelevant

[22],*[16]* - data_format

Table 40: [22],*[16]* - data_format

Bit	Function	Default	Comment
[1:0]	Unused	1	
2	Line read-out order (vertical) **Unshuffled** or Shuffled	0	If the line read out is shuffled, all the even address rows are read out first followed by all the odd address rows
3	Pixel read-out order (hmirror) **Normal** or Mirrored	0	If the pixel read out is horizontally mirrored, the columns are read out in reverse order, that is the column on the right of the sensor array appear on the left of the displayed image and vice versa
4	Line read-out order (vertical flip) **Normal** or Mirrored	0	If the line read out is vertically mirrored, the rows are read out in reverse order, that is the row at the bottom of the array appears at the top of the displayed image and vice versa.
5	FST/LST **Enable**/Tri-state	0	The FST/LST digital outputs can be tri-stated but are enabled as outputs by default. FST/LST enabling/ disabling is retimed to a field boundary. The state of this control bit is always available via a I^2C read, i.e. it does not have to wait to change state at a field boundary
6	QCK **Enable**/Tri-state	0	The QCK output can be tri-stated independently. The enabling/disabling of QCK can be retimed to a field boundary. The state of this control bit is always available via a I^2C read, i.e. it does not have to wait to change state at a field boundary.
7	Pre clock generator divide On/**Off**	0	The CIF and QCIF video modes expect a recommended set of input clock frequencies, however the acceptable range of clock frequencies can be extended if this bit is set. If this bit is set , the primary input clock is divided down by 1.5 prior to the clock generator, thus if the expected clock input is 16 MHz, we can set this bit and accept 24 MHz and achieve the same final frame rate.

Table 41 : FST/LST output control

OEB pin	data_format[5]	oeb_composite	Comments
0	0	0	FST/LST outputs enabled.
0	1	1	FST/LST outputs are tri-stated by data_format[5]
1	0	1	FST/LST outputs are tri-stated by OEB pin.
1	1	1	FST/LST outputs are tri-stated.

Table 42 : QCK output control

OEB pin	data_format[6]	oeb_composite	Comments
0	0	0	QCK output enabled.
0	1	1	QCK output is tri-stated by op_format[6]
1	0	1	QCK output is tri-stated by OEB pin.
1	1	1	QCK output is tri-stated.

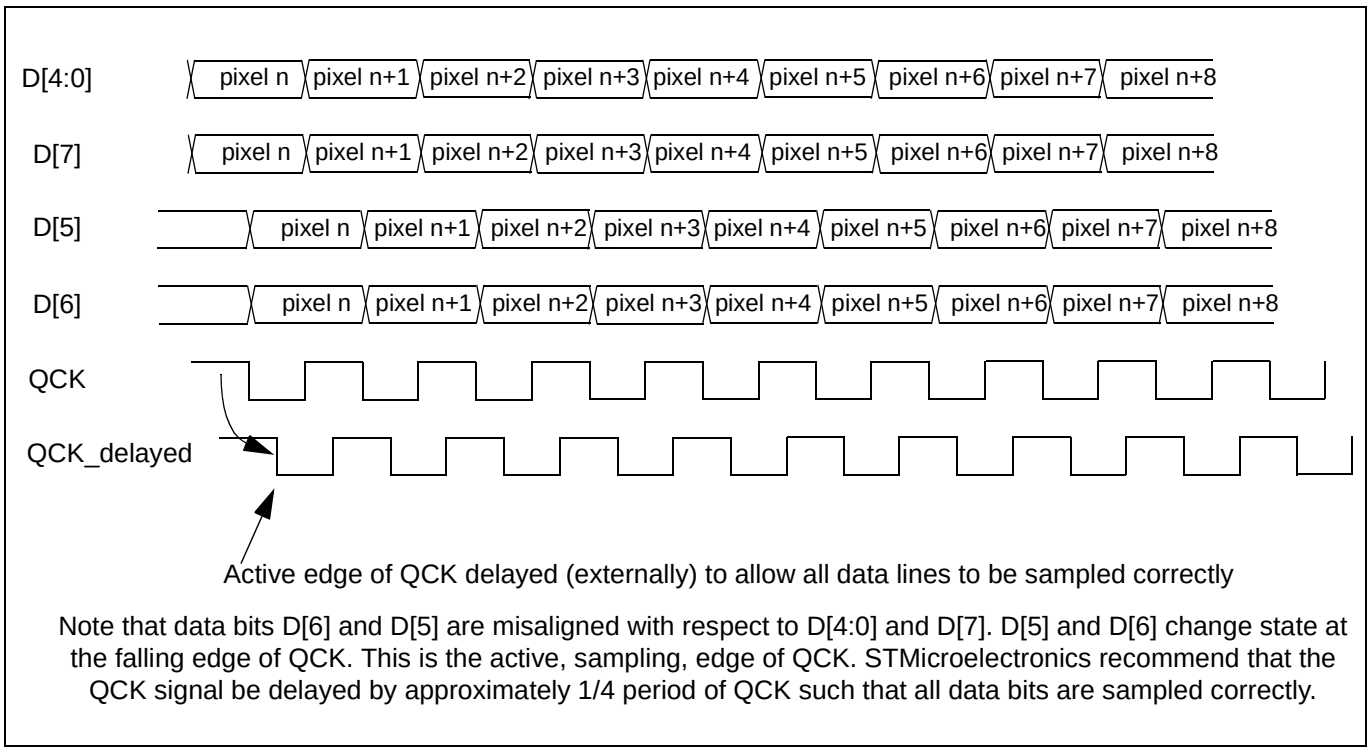
[23],*[17]* - op_format

Table 43 : [23],*[17]* - op_format

Bit	Function	Default	Comment
1:0	Data format select.	0	00 - 5 wire parallel output 01 - 4 wire parallel output 1x - 8 wire parallel output Note: If the 8 wire output option has been selected then the FST and LST pins will output data bits 5 and 6 respectively, normal FST and LST function is not available
2	Embedded SAV/EAV escape sequences[a] **On /** Off	0	0 - Insert Embedded Control Sequences e.g Start and End of Active Video into Output Video data 1 - Pass-through mode. Output Video data equals ADC data.
4:3	Reserved	11	
5	Tri-state output data bus **Enabled** / Tri-state	0	On power up the data bus pads are enabled by default. This bit is OR'ed with the OEB pin to generate the enable signal for the data pins as detailed in Table 44
6	Re-time tri-state update. **Off** / On	0	Re-time new tri-state value to a field boundary. This bit affects the updating of the op_format[5] as well as data_format[6:5]
7	unused	0	

a. Please note that if the embedded coding sequences are disabled then the FST signal is also disabled. The QCK output will continue to function IF the free running option has been selected. The LST functionality is unaffected by the state of this bit.

Figure 38: Detailed timing in 8-bit output mode



Note that data bits D[6] and D[5] are misaligned with respect to D[4:0] and D[7]. D[5] and D[6] change state at the falling edge of QCK. This is the active, sampling, edge of QCK. STMicroelectronics recommend that the QCK signal be delayed by approximately 1/4 period of QCK such that all data bits are sampled correctly.

Table 44 : Data bus output control

OEB pin	op_format[5]	oeb_composite	Comments
0	0	0	Data outputs enabled.
0	1	1	Data outputs are tri-stated by op_format[5]
1	0	1	Data outputs are tri-stated by OEB pin.
1	1	1	Data outputs are tri-stated.

Note: oeb_composite is the logical OR of op_format[5] and the OEB pin.

[24],*[18]* - mode_select

This register allows the user to configure the sensor to operate with the present generation of coprocessors as well as anticipated future devices.

Table 45 : [24],*[18]* - mode select

Bit	Function	Default	Comment
0	Coprocessor device is VP3 No/**Yes**	1	By default, the sensor expects the coprocessor to be a VP3 device. If the sensor is not used with a VP3 device this bit should be reset. This bit controls the arrangement of black/dark/visible lines within the field. It does not alter timing. Please see *Figure 14* to *Figure 26* for more details.
1	Retro mode for gain application **Off**/On	0	The gain passed to the CAB comprises 2 components, IDAC[3:0] (the ls nibble of the gain register, index 0x'24) and CDAC[5:0] (the msnibble of the gain register, index 0x'24). If the user selects the retro mode then the IDAC value will be the inverse and reverse of the ls gain nibble. If the retro mode is not selected then the IDAC value will simply be the inverse of the ls gain nibble. The user is barred from writing to the ms gain nibble in retro mode. In the non retro mode, all 8 bits are available to program. The 2 ls bits of CDAC[5:0] are fixed at 2'b11. The remaining bits should be programmed to 4'b1111 to ensure optimal device performance.
2	Select log CDAC ramp **Off**/On	0	By default the same CDAC value is applied for the duration of every line of every field. Setting this bit causes the CDAC value to vary during the line.
[7:3]	Reserved		

[25-31],*[19-1F]* - unused

8.2.6 Exposure control registers [32 - 47],*[20-2F]*

A set of programmable registers controls the sensor sensitivity. These registers are:

- Fine exposure.
- Coarse exposure.
- Analog gain.
- Clock division

Note: As explained earlier in this document (see Chapter 5 in page 25), exposure control registers are not immediately updated, they are timed to be updated at a precise point in the field timing.

The range of some parameter values is limited and any value programmed out-with this range will be clipped to the maximum currently permitted, (the fine and coarse maximum allowable settings are set by the current line and field length respectively).

Table 46: Exposure related registers

$Index_{10}$	$Index_{16}$	Bits	Function	Default	Comment
32	20	0	Fine MSB exposure value	0	The maximum fine exposure is line length dependent. The expressions used to calculate the maximum fine exposure for each of the default video modes selectable via Setup0 register are: NTSC = line length - 51 PAL = line length - 86 CIF = line length - 51 QCIF = line length - 23
33	21	[7:0]	Fine LSB exposure value		
34	22	0	Coarse MSB exposure value	302	The maximum allowable coarse exposure setting is filed- length dependent. We provide the maximum coarse exposure settings for each of the standard video modes. NTSC = 260 PAL = 310 CIF (25 & 30 fps) = 318 QCIF (25 & 30 fps) = 158
35	23	[7:0]	Coarse LSB exposure value		
36	24	[7:0]	Analog gain value	1111_0000	Bits [7:4] CDAC gain control CDAC default = 63 (10-bit modes) CDAC default = 31 (9-bit modes) Bits[3:0] IDAC maximum recommended IDAC value = 12.
37	25	[3:0]	Clock divisor value	0	The user can opt to slow the internal clocks down form their default settings. Table 47 describes the range of clock divisors that may be selected.

Table 47 : Clock divisor values

Clock divisor setting	Pixel clock divisor
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

[38-43],*[26-3B]* - reserved

[44 - 45],*[3C-3D]* - Dark pixel offset

Table 48 : [44 - 45],*[3C-3D]* - Dark pixel offset

Bit	Function	Default	Comment
[2:0]	MS Dark line pixel offset	0	This register contains a fixed offset that can be applied to the digitized pixels in the digital output coding block. The offset is a 2’s complement number, giving an offset range -1024,+1023. If this external offset cancellation is to be applied then it register[46], bits[1:0] should be reprogrammed to 2’b1x.
[7:0]	LS Dark line pixel offset		

[46],*[3E]* - Dark Pixel Cancellation Setup Register

Table 49: [46],*[3E]* - Dark pixel cancellation setup register

Bit	Function	Default	Comment
[1:0]	Dark line offset cancellation	01	x0 - Accumulate dark pixels, calculate dark pixel average and report, but don't apply anything to data stream **01** - Accumulate dark pixels, calculate dark pixel average and report and apply internally calculated offset to data stream 11 - Accumulate dark pixels, calculate dark pixel average and report, but apply an externally calculated offset
2	Number of dark lines used **All dark lines**/Use half the number of dark lines.	0	The dark line offset cancellation algorithm can opt to only use pixels from dark lines that are preceeded by another dark line, i.e line choose only line 306 from line 305 and line 306.
[5:3]	reserved		
6	Use narrow dark offset deadband **Yes**/No	1	The deadband describes a range of dark pixel averages that will force the leaky integrator algorithm to hold it's current value. 0 - Target +/- 4 codes 1 - Target +/- 2 codes
7	unused	0	

[47],*[3F]* - reserved

[48-79],*[30-4F]* - reserved

8.2.7 Video timing registers [80 _ 103],*[50-67]*

Indexes in the range [80 - 103] control the generically named video timing registers, including the image pan/tilt parameters and line & field length of the sensor. The registers are the following:

1 line length.
2 x-offset of region of interest.
3 y-offset of region of interest.
4 frame length.

The length of a line is specified in a number of pixel clocks, whereas the length of a field is specified in a number of lines.

The range of some parameter values is limited and any value programmed out with this range will be clipped to the maximum allowed. The x-offset and y-offset are only programmable if the user has selected the pan tilt QCIF mode. If the other video modes are selected, the x-offset and y-offset registers have pre-programmed values that cannot be changed. The x-offset and y-offset default values are chosen so that the output image, regardless of video mode selected, is centered within the pixel array, (see Section 2.2 for details).

Table 50: Video timing registers

$Index_{10}$	$Index_{16}$	Bit	Function	Default	Comment
80-81	50-51		reserved		
82	52	[1:0]	Line Length MSB value	415	Minimum mode dependent Maximum = 1023 Actual line duration in pixel periods is line length programmed +1.
83	53	[7:0]	Line Length LSB value		
84 - 86	54-56		reserved		
87	57	0	x-offset MSB value	5	Minimum (positive) value = 1
88	58	[7:0]	x-offset LSB value		
89	59	0	y-offset MSB value	3	Minimum (positive) value = 1
90	5A	[7:0]	y-offset LSB value		
91 - 96	5B-60		reserved		
97	61	[1:0]	Field Length MSB value	319	Minimum mode dependent Maximum = 1023 Actual field duration in line periods is field length programmed +1.
98	62	[7:0]	Field Length LSB value		
99-102	63-66		reserved		

[103],*[67]* - unused

[104-105],*[68-69]* - reserved

[106-107],*[6A-6B]* - unused

[108-109],*[6C-6D]* - reserved

[110-111],*[6E-6F]* - unused

8.2.8 System registers addresses [112 - 127],*[70-7F]*

This page of the I^2C address space comprises a wide range of registers including the registers required to control the black offset cancellation algorithm, enable test modes and also control various aspects of the analogue behavior of the sensor.

[112 - 113],*[70-71]* - Black pixel offset

Table 51 : [112 - 113],*[70-71]* - Black pixel offset

Bit	Function	Default	Comment
[2:0]	MS Black line pixel offset	- 64	This register contains a fixed offset that can be applied to the digitized pixels in the digital output coding block.The offset is a 2's complement number, giving an offset range -1024,+1023. If this external offset cancellation is applied, its register[114], bits[1:0] should be reprogrammed to 2'b1x.
[7:0]	LS Black line pixel offset		

[114],*[72]* - Black pixel cancellation setup register

Table 52: [114],*[72]* - Black offset cancellation setup

Bit	Function	Default	Comment
[1:0]	Black line offset cancellation	01	x0 - Accumulate black pixels, calculate black pixel average and report, but don't apply anything to data stream **01** - Accumulate black pixels, calculate black pixel average and report and apply internally calculated offset to data stream 11 - Accumulate black pixels, calculate black pixel average and report, but apply an externally calculated offset
[4:2]	reserved	100	The time constant controls the rate at which a change in the black level is corrected.
5	Use narrow black offset deadband **Yes**/No	1	The deadband describes a range of pixel averages that causes the leaky integrator algorithm to hold it's current value. 0 - Target +/- 4 codes 1 - Target +/- 2 codes
[7:6]	unused	00	

[115],*[73]* - unused

[116],*[74]* - reserved

[117 - 118],*[75-76]* - Control registers 0 and 1- CR0 and CR1

Although we give the user access to the following 5 registers, it is possible that their content is altered. If the user wishes to alter any of the register bits then they are strongly advised to contact VIBU prior to doing so.

Table 53: [117],*[75]* - Control register CR0

Bit	Function	Default	Comment
0	Enable bit line clamp: Off/On	0	
1	Enable bit line test: Off/On	0	
3:2	Bit line white reference 0.7 V / 1.1 V / 1.5V / Ext.	00	00 - 0.7V 01 - 1.1V 10 - 1.5V 11 - External
4	Enable anti blooming: Off/On	0	
5	Power Down - LVDS input comparator: Off/On	0	Powers down LVDS input. CMOS clock input may still be used.
6	Power Down - SRAM: Off/On	0	Powers down SRAM comparator
7	Power Down - VCCS: Off/On	0	Powers down voltage controlled current source

Table 54: [118],*[76]* - Control register CR1

Bit	Function	Default	Comment
0	Stand-by **Off**/On	0	Powers down ALL analog circuitry with the exception of the band gap
1	Power Down - Internal Ramp Generator **Off**/On	0	
2	Power Down - Column ADC **Off**/On	0	Powers down preamp and comparators
3	Power Down - CAB regulator **Off**/On	0	Referred to in figures as pd_creg
4	Power Down - Audio Amplifier regulator **Off**/On	0	Referred to in figures as pd_areg
5	Power Down - VRT Amplifier **Off**/On	0	Allows external VRT to be applied
6	Ramp common mode voltage **VRT-vtn**/1.5V	0	0 - VRT-vtn ramp common mode voltage 1- 1.5V ramp common mode voltage
7	Current boost to column comparator **75uA**/50uA	0	0 - 75uA 1- 50uA

[119]*[77]* - ADC setup register AS0

Table 55: [119],*[77]* - ADC setup register AS0

Bit	Function	Default	Comment
[1:0]	reserved	10	
2	Enable voltage doubler **Off**/On	0	It is recommended that this bit is set if the sensor is being used in a 3.3V supply environment
3	Differential ramp enable Off//**On**	1	Ramp generator signal bpramp
4	view column/view vcmtcas **vcmtcas**/column	1	0 - view column voltage Vx[363] 1- view vcmtcas
5	ramp viewing/column comparator test **ramps**/test comparator	0	0 -view ramps on CPOS/CNEG 1- input to test comparator 364
6	Stepped Ramp Enable Off**/On**	1	Setting this bit enables a stepped ramp. Clearing this bit enables a continuous ramp.
7			

[120],*[78]* - Analog test register AT0

Table 56: [120],*[78]* - Analog test register AT0

Bit	Function	Default	Comment
0	SRAM test enable **Off**/On	0	
[2:1]	VRT Voltage **2.2V** / 2.5V / 2.8V / Ext.	00	**00** - VRT = 2.2V 01 - VRT = 2.5V 10 - VRT = 2.8V 11 - reserved
[4:3]	LineInt & ReadInt phasing	00	**00**- 0 degree phase delay 01 - 90 degree phase delay 10 - 180 degree phase delay 11 - 270 degree phase delay
[7:5]	unused	000	

[121],*[79]* - Audio amplifier setup register AT1

Table 57: [121],*[79]* - Audio amplifier setup register AT1

Bit	Function	Default	Comments
0	Gain options	1	0 - 0dB 1 - 27dB[a]
[2:1]	Unused		
3	Power Down	0	0 - Powered up 1 - Power down
4	Output Select	0	0 - Single ended 1 - Differential
5	Current Boost	0	0 - 1mA output drive in output buffers 1 - 2mA output drive in output buffers
7:6	Unused		

a. This is a mean value. 29dB is the max value guaranteed by test. Overall spread of +/- 2dB from mean.

[122-125],*[7A-7D]* - unused

[126-127],*[7E-7F]* - reserved

8.3 Types of messages

This section gives guidelines on the basic operations to read data from and write data to the I^2C.

The I^2C supports variable length messages. A message may contain no data bytes, one data byte or many data bytes. This data can be written to or read from common or different locations within the sensor. The range of instructions available are detailed below.

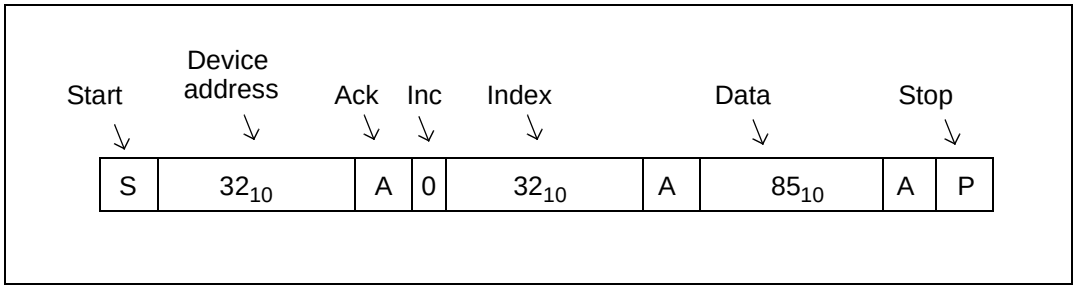
- Write no data byte, only sets the index for a subsequent read message.
- Single location data write or read for monitoring (real time control)
- Multiple location read or write for fast information transfers.

Examples of these operations are given below. A full description of the internal registers is given in the previous section. For all examples the slave address used is 32_{10} for writing and 33_{10} for reading. The write address includes the read/write bit (the lsb) set to zero while this bit is set in the read address.

8.3.1 Single location, single data write

When a random value is written to the sensor, the message looks as shown in *Figure 39*.

Figure 39: Single location, single write

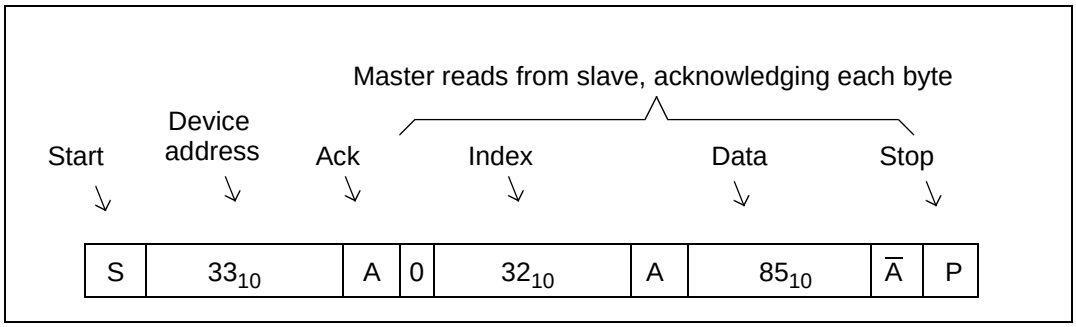


In this example, the *fineH* exposure register (index = 32_{10}) is set to 85_{10}. The r/w bit is set to zero for writing and the *inc* bit (msbit of the index byte) is set to zero to disable automatic increment of the index after writing the value. The address index is preserved and may be used by a subsequent read. The write message is terminated with a stop condition from the master.

8.3.2 Single location, single data read

A read message always contains the index used to get the first byte.

Figure 40: Single location, single read



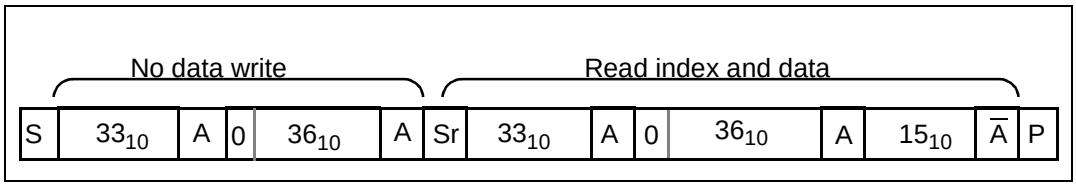
This example assumes that a write message has already taken place and the residual index value is 32_{10}. A value of 85_{10} is read from the *fineH* exposure register. Note that the read message is terminated with a negative acknowledge ($\overline{A}$) from the master: it is not guaranteed that the master will be able to issue a stop condition at any other time during a read message. This is because if the data sent by the slave is all zeros, the *sda* line cannot rise, which is part of the stop condition.

8.3.3 No data write followed by same location read

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master, a repeated start

condition is asserted between the write and read messages, i.e. no stop condition is asserted. In this example, the *gain* value (index = 36_{10}) is read as 15_{10}:

Figure 41: No data write followed by same location read



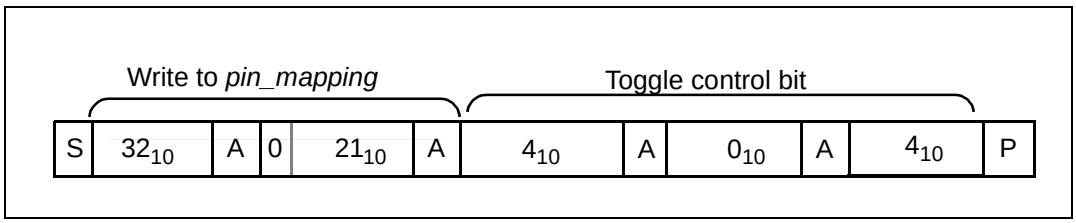
As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

8.3.4 Same location multiple data write

It may be desirable to write a succession of data to a common location. This is useful when the status of a bit (e.g. auto-load) must be toggled.

The message sequence indexes *sf_setup* register 108. If bit 0 is toggled high, low this will initiate a fresh auto-load. This is achieved by writing two consecutive data bytes to the sensor. There is no requirement to re-send the register index before each data byte.

Figure 42: Same location multiple data write

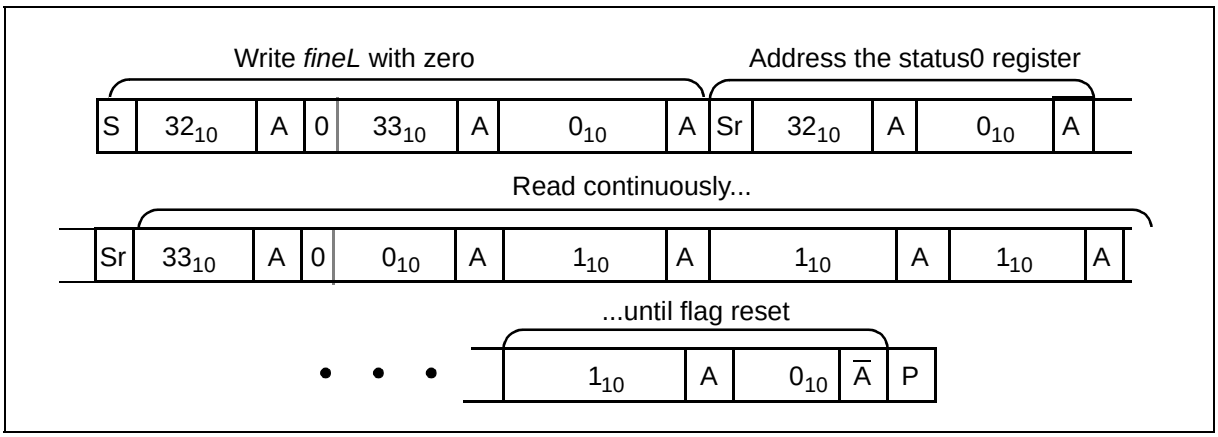


8.3.5 Same location multiple data read

When an exposure related value (*fineH, fineL, coarseH, coarse L*, *gain or clk_div*) is written, it takes effect on the output at the beginning of the next video frame, (remember that the *gain* value is applied a frame later than the other exposure parameters). To signal the consumption of the written value, a flag is set when any of the exposure or gain registers are written and is reset at the start of the next frame. This flag appears in *status0* register and may be monitored by the bus master. To speed up reading from this location, the sensor will repeatedly transmit the current value of the register, as long as the master acknowledges each byte read.

In the following example, a *fineH* exposure value of 0 is written, the status register is addressed (no data byte) and then constantly read until the master terminates the read message.

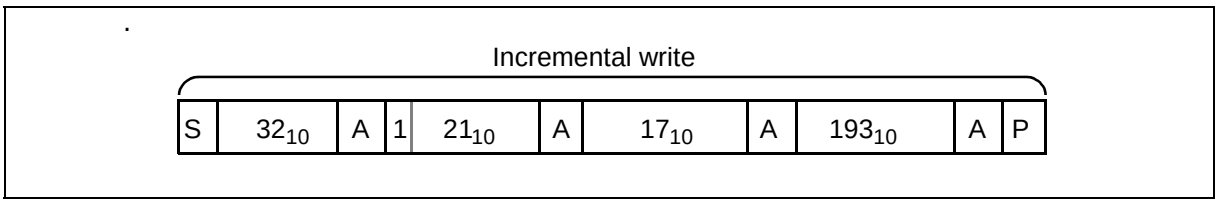
Figure 43: Same location multiple data read



8.3.6 Multiple location write

If the automatic increment bit is set (msb of the index byte), it is possible to write data bytes to consecutive adjacent internal registers, (i.e. 23,24,25,26 ect), without having to send explicit indexes prior to sending each data byte. An auto-increment write to the exposure registers with their default values is shown in the following example, where we write 17_{10} to the pin_mapping register[21] and 193_{10} to the data format register[22].

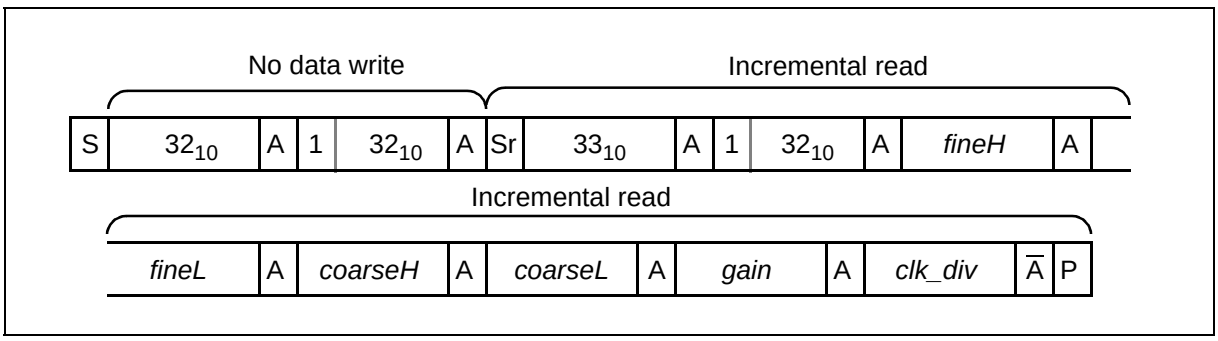
Figure 44: Multiple location write



8.3.7 Multiple location read

In the same manner, multiple locations can be read with a single read message. In this example the index is written first, to ensure the exposure related registers are addressed and then all six are read.

Figure 45: Multiple location read



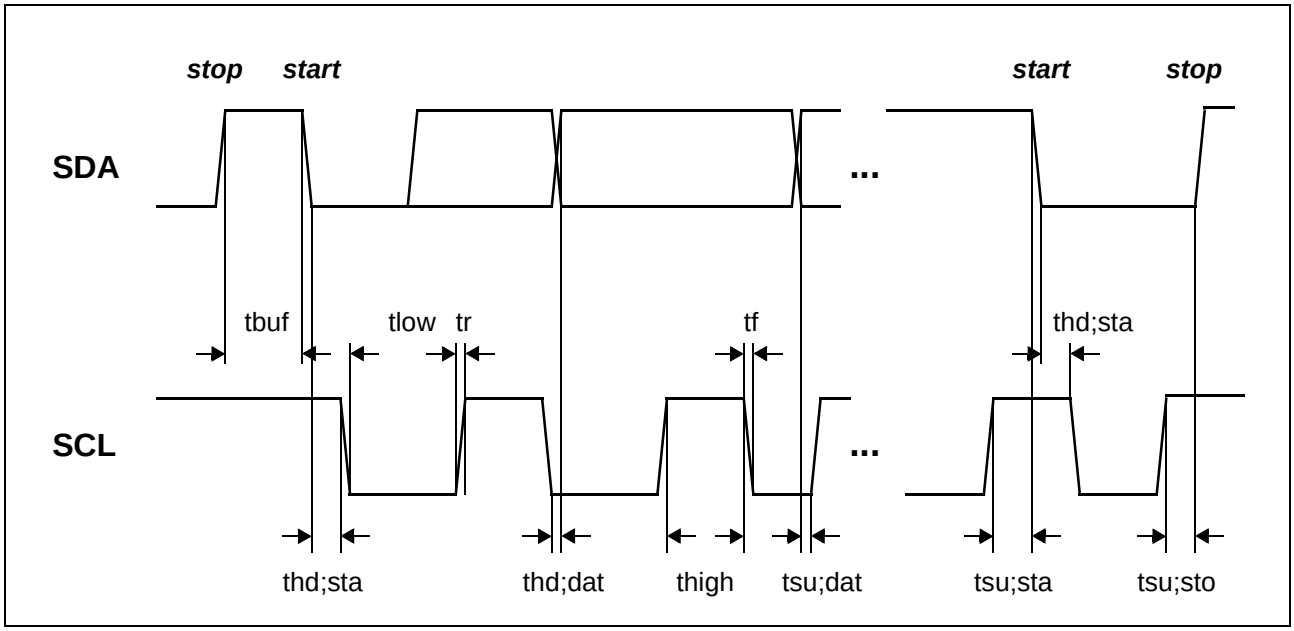
Note: A stop condition is not required after the final negative acknowledge from the master, the sensor will terminate the communication upon receipt of the negative acknowledge from the master.

8.4 I²C timing

Table 58: I²C timing characteristics

Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	fscl	0	100	kHz
Bus free time between a ***stop*** and a ***start***	tbuf	2	-	us
Hold time for a repeated ***start***	thd;sta	80	-	ns
LOW period of SCL	tlow	320	-	ns
HIGH period of SCL	thigh	160	-	ns
Set-up time for a repeated ***start***	tsu;sta	80	-	ns
Data hold time	thd;dat	0	-	ns
Data Set-up time	tsu;dat	0	-	ns
Rise time of SCL, SDA	tr	-	300	ns
Fall time of SCL, SDA	tf	-	300	ns
Set-up time for a ***stop***	tsu;sto	80	-	ns
Capacitive load of each bus line (SCL, SDA)	Cb	-	200	pF

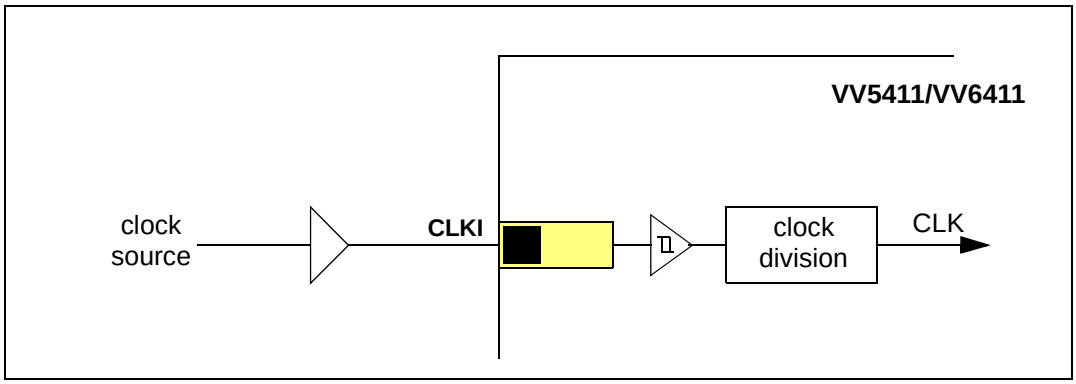
Figure 46: I²C timing characteristics



9 Clock Signal

VV5411/VV6411 system clock is supplied by an external clock source that irectly drives the CLKI pin. The clock pad has an integral Schmitt buffer to filter noise from the clock source. Please note that there is no support for an external resonator circuit.

Figure 47: CMOS clock source



The clock signal must be a square wave with, ideally a 50% (±10%) mark/space ratio, although a non-ideal mark/space ratio can be tolerated, please contact STMicroelectronics for details. The maximum input clock frequency for the module is 24.0 MHz. If the 24MHz crystal is preferred then the user must select the pre-clock-divide-by-1.5 option so that the bulk of the internal logic is driven by a 16MHz clock, see I^2C, register 16_{10}, data_format.

10 Other Features

10.1 Audio amplifier

VV5411/VV6411 contains an on-chip audio amplifier which can be configured via the I^2C. The amplifier can also be powered down via the I^2C.

The following document outlines the implementation of audio circuitry on the VV5411/VV6411 sensor.

10.2 Audio amplifier configuration

The audio circuit is controlled through a single eight bit register on the VV5411/VV6411. This includes bits for power down, output select, gains and current boosting. *Table 59* describes the functionality of the control register bits.

The audio amplifier provides a gain of 0dB or 29dB using a low noise design. The reference is provided from the on-chip bandgap voltage.

Table 59: Control register summary for VV5411/VV6411 audio circuit.

Bit	Function	Default	Comments
0	Gain options	1	0 - 0dB 1 - 27dB[a]
2:1	Unused		
3	Power Down	0	0 - Powered up 1 - Power down
4	Output Select	0	0 - Single ended 1 - Differential
5	Current Boost	0	0 - 1mA output drive in output buffers 1 - 2mA output drive in output buffers
7:6	Unused		

a. This is a mean value. 29dB is the max value guaranteed by test. Overall spread of +/- 2dB from mean.

The output of the inverting gain stage may be routed through the other output buffer to provide two single ended outputs. Otherwise, the inverted and non-inverted outputs provide a fully differential output signal.

Further circuit specifications are given in *Table 60*.

10.2.1 AUD3V3 (audio supply regulator)

Table 60: Audio circuit specification

Symbol	Parameter	Min	Typical	Max	Units
AUD3V3	Regulated supply (No external load)	2.79	3.1	3.41	V
AUD3V3_Ld	Regulated supply Vdrop (Current Load 20mA)		-50		mV
AUD3V3_sus	Regulated supply (Suspend mode)		Off		V
PSRR	Power Supply Rejection versus Vin		-38		dB
THD	Total harmonic distortion		<0.1		%

10.2.2 Audio amplifier parameters

Table 61: Audio amplifier parameters

Symbol	Parameter	Min	Typical	Max	Units
VAin	Audio Regulator Input Voltage		V_{bg}		V
R_{IN}	Input impedance		100		kΩ
Gain	Gain accuracy		+/-2.0		dB
Gmatch	Differential output mode gain matching (0dB) (27dB)		 0.2 0.5		dB
Out_max	Output Clipping Level[a]	1.6	2.2		Vpp
OUT_DC	Output DC Voltage	1.1	1.22	1.3	V
D-OUT_DC	Differential DC Offset (AoutN-AoutP)		20	100	mV
Rout	Output Impedance		2		kΩ
THD	THD (includes noise) Vin = 20mVpp, f-1KHz, Gain =27dB		0.2		%
SNR	Signal to Noise ratio (1KHz) (10KHz)[b]		 65 75		dB
PSRR	Power supply rejection ratio from Vin		-55		dB
LFc	Low frequency cutoff (Cin=100nF)		15		Hz
Xtalk	Video crosstalk to audio outputs (gain = 27dB)		-56		dB

a. Minimum dynamic range includes dcout (i.e. Vclip- OUT_DC is greater than Vppmin/2)

b. Assumes 10µF bypass capacitors on all supplies and well separated supplies and grounds

10.2.3 Audio amplifier bandwidth[1]

The audio circuit bandwidth can be limited to a first order through the use of minimum external circuitry. The two outputs, AoutP and AoutN, require compensation capacitors that can also be used to define the circuit bandwidth.

Table 62: Compensation capacitor values

Compensation capacitor (nF)	3dB bandwidth	Units
1	175	kHz
10	41	kHz
100	4.2	kHz

Finaly, the addition of a resistor (microphone biasing) and a decoupling capacitor at the input permits the realization of a first order high-pass filter. This can easily be designed to remove frequencies below 50Hz/60Hz (main electricity noise).

10.3 Voltage regulators

VV5411/VV6411 contains three on-chip voltage regulators, among which two can be powered-down via the I^2C. The third regulator that controls the band gap references is never powered down. The band gap circuitry consumes extremely low power (only 30µA).

10.3.1 Regulator for digital system

If an external bipolar is populated, as represented in *Figure 49*, a voltage regulator is realized. This regulator, with Reg3V3 as an output, powers the digital logic and can also power an external co-processor/other device. The regulator can source a load from 300µA -> 300mA and regulate up to 3.0V ± 10% from an input range of 4-6V. If the VV5411/VV6411 is set into the USB compatible suspend mode and if the input clock to the digital logic is removed, the power consumption is limited to less than 100µA. If an external 3.3V supply is available, this regulator can be overdriven by an external 3.3V supply to directly power the logic.

10.3.2 Regulator for video supply/analogue core

Vid3V3, the regulator output for the video supply, powers the analog core. This regulator can be powered-down via the serial interface but is powered up by default. Note that the sensor is in low power mode initially.

10.3.3 Valid supply voltage configurations

The power supplies to the VV5411/VV6411 sensors can be configured so that the sensor operates in a number of systems:

- Nominal 5V supply. Sensor regulates 3V3 internally with optional BJT to satisfy current demand.
- Direct drive the sensor with 3V3 (internal voltage regulators are powered down in this mode).

See *Figure 48* and *Figure 49* for details about the options described here above.

1. Each audio output must have a capacitor (Ccomp) connected to ground to avoid any oscillation

Figure 48: USB power setup

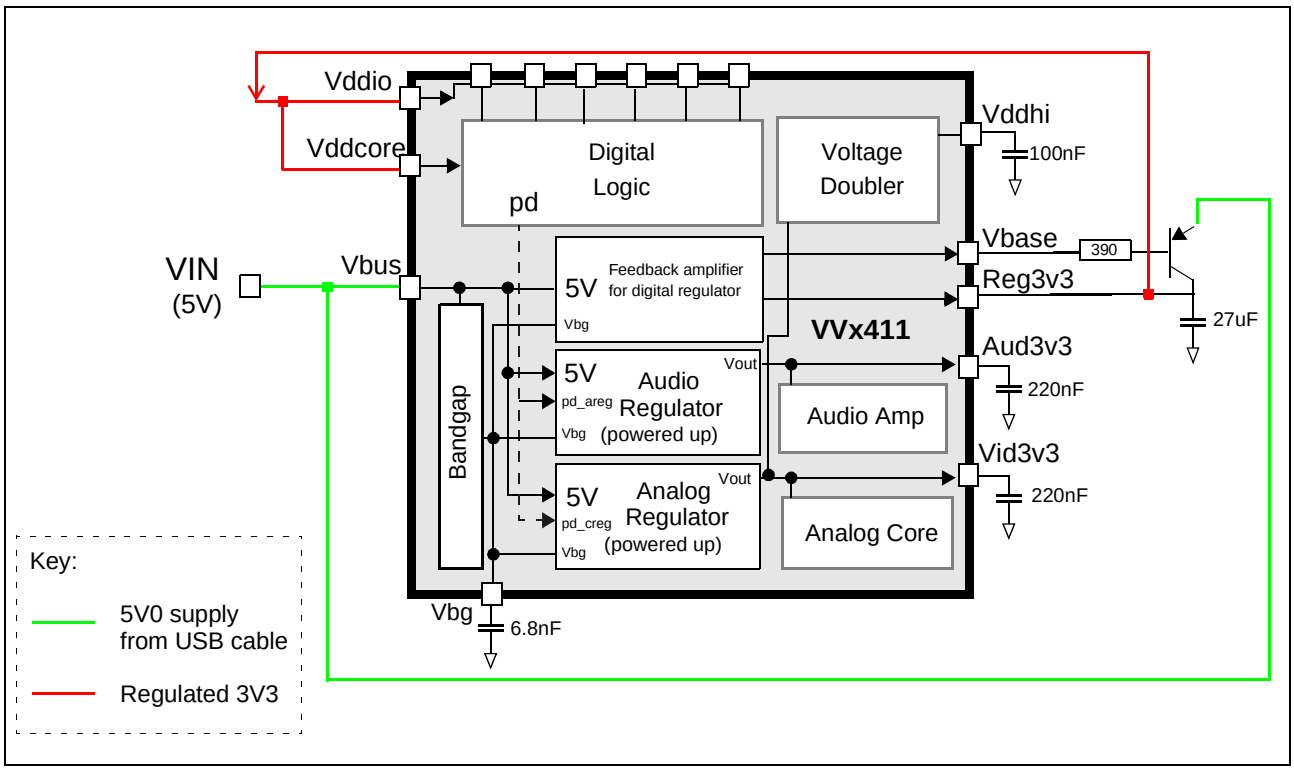


Figure 49: Direct drive @3V3 Setup

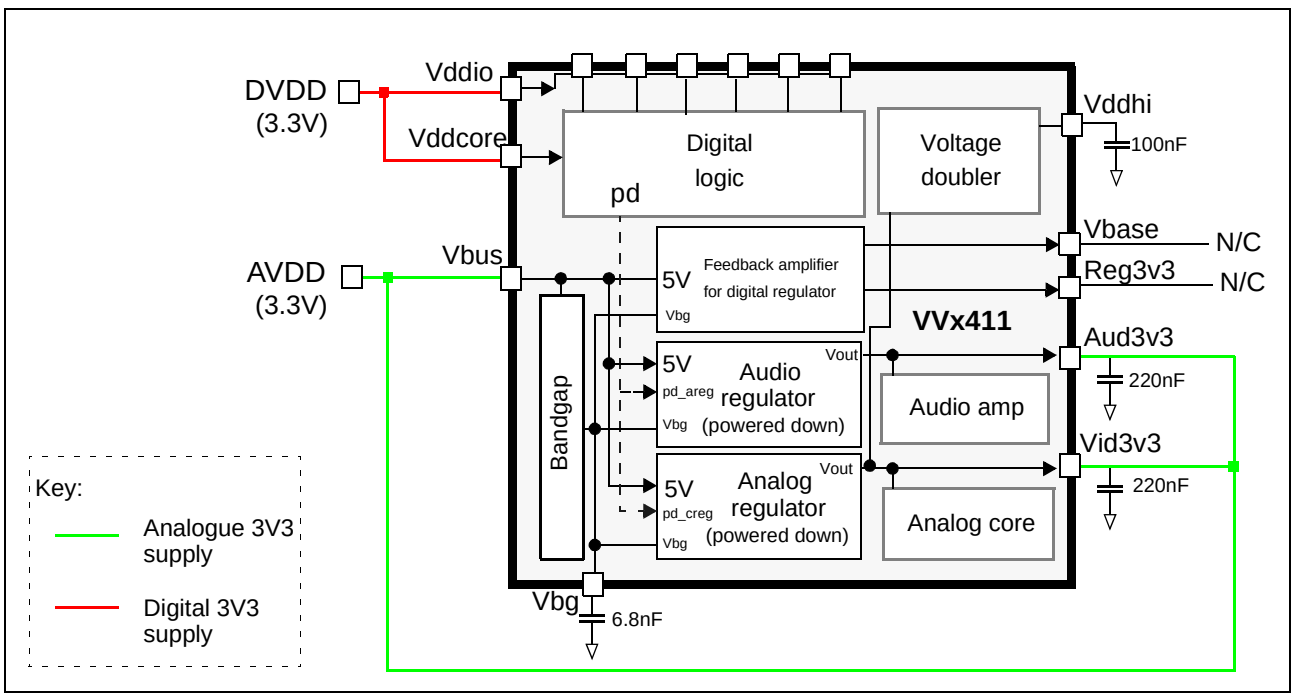


Table 63: Sensor voltage supply summary

Supply	USB System	3.3V-only System
Vbus	Supply from USB cable	3.3V direct drive
Vddio	connect to Vreg3v3	3.3V direct drive
Vddcore	connect to Vreg3v3	3.3V direct drive
Reg3v3	BJT populated	BJT not populated
Vid3v3	generated by internal regulator	internal regulator powered down
Aud3v3	generated by internal regulator	internal regulator powered down

10.4 Programmable pins

The FST and QCK pins can be re-configured to follow the values of bits 1 and 2 in the I^2C register *pin_mapping*. This permits the remote control of a electro-mechanical system, maybe two different crop settings, in a remote camera head via the I^2C.

11 Characterization Details

11.1 VV5411/VV6411 AC/DC specification

Table 64: VV5411/6411 DC specification

Parameter	Comment	Units
Exposure control range	81 (minimum exposure period: 3µs maximum exposure period: 33ms)[a]	db
Supply Voltage	3.0-6.0 DC +/-10%	V
Operating Temp. range	0 - 40	^{o}C
V_{OL_max}[b]	0.8	V
V_{OH_min}[c]	2.0	V
V_{IL_max}[d]	1.2	V
V_{IH_min}[e]	2.0	V
I^2C frequency range	up to 100	kHz
ESD (Human body model)	Class500[f]	V

a. We assume CIF (30fps) mode, input clock of 16MHz and internal clock divisor of 1.

b. This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 3V0

c. This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 3V0

d. This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 3V0

e. This is worst case reading. Device outputs had significant capacitive loading and supply voltage reduced to 3V0

f. A Class500 device can withstand up to 500V on package pins

11.2 VV5411/VV6411 optical characterization data

Table 65 : VV5411/VV6411 optical characterisation data (typical)

Optical parameter	Min	Typical	Max	Units
Dark Signal	-	67	-	mV/sec
Average Sensitivity	-	2.75	-	V/lux.sec
Fixed Pattern Noise (FPN)	-	1.03	-	mV
Vertical Fixed Pattern Noise (VFPN)	-	0.53	-	mV
Random Noise	-	1.7	-	mV
Sensor SNR	-	c.56	-	dB
Shading (Gross)	-	0.42	-	mV

11.2.1 Noise parameters and dark signal

Various noise parameters are measured on the V5411/V6411 device as follows:

- Fixed Pattern Noise (FPN)
- Vertical Fixed Pattern Noise (VFPN)
- Random Nnoise
- Fine shading
- Gross shading

The parameters are detailed in the following pages, along with the data produced by the characterization programme.

11.2.2 Blooming

Blooming is a phenomenon that does not affect CMOS sensors the same way as CCD imagers are afflicted. CCD blooming can cause an entire column/columns to flood and saturate.

CMOS imagers are however affected by a different type of saturation. If an intense light source is shone very close to the image sensor, the pixel sampling mechanism breaks down and displays a black image rather than a saturated white light.

The 411 pixel architecture uses Correlated Double Sampling (CDS) to reduce noise in the system. The pixel is read normally first, yielding the true integrated signal information, then the pixel is reset and very quickly read for a second time. This normally yields black information - as the pixel has had no exposure time - that can be subtracted from the signal from the first read. This subtraction will remove much of the noise from the pixel, leaving only the useful signal information.

If for example a pixel is saturated in both the first and the second reads due to an intense light source, the result from the noise cancellation subtraction operation is close to a zero signal from the pixel. Therefore, the resulting displayed image is black.

We do not perform any test measurements for this phenomenon.

11.2.3 Dark signal

This is defined as the rate at which the average pixel voltage increases over time when the device is not illuminated. The dark signal measured at a gain setting of 4, a clock divisor of 16 at a fixed temperature is expressed in mV.

11.2.4 Fixed pattern noise

The FPN of an image sensor is the average pixel non-temporal noise divided by the average pixel voltage. The illumination source is the IR filtered-white light producing a diffuse uniform illumination at the surface of the sensor package. The FPN is calculated at coarse exposure settings of 0,10,150,250 and 302 with a gain set to 1. 10 frames are grabbed and averaged to produce a temporally independent frame before each calculation. FPN is expressed in mV.

11.2.5 Vertical fixed pattern noise

VFPN describes the spatial noise in an image sensor related to patterns with a vertical orientation. The VFPN is defined as the standard deviation over all columns of the average pixel voltage for each column determined at zero exposure and zero illumination. VFPN is expressed in mV.

11.2.6 Random noise

Random noise is the temporal noise component within the image. Random noise is expressed in mV.

11.2.7 Shading

This describes how average pixel values per “block” change across the image sensor array. For fine shading calculations, the image sensor array is split into 30 pixel by 30 pixel blocks. An average value is then calculated for each block, averages are then compared across the whole device. The blocks are increased in size to 60 pixels by 60 pixels for the gross shading calculation. Shading is expressed in mV.

11.3 VV5411/VV6411 power consumption

Table 66: VV5411/6411 Current consumption in different modes

Operating condition	Current consumption
Low power mode current consumption	<8mA
Sleep mode current consumption[a]	<20mA
Suspend mode current consumption (with CLKIP disabled)	<100uA
Normal operating mode current consumption[b]	<40mA

a. Estimated figures - this parameter was not measured during final characterization

b. Measured while device is clocked at 16MHz and streaming CIF video at 30fps

11.4 Digital input pad pull-up and pull-down strengths

Table 67 : Pad pull-up/pull-down strengths

Pad type	Pads	Min current	Max current
Library pulldown	oeb	35 µA	52 µA
Library pullup	scl, sda, suspend	25 µA	42 µA
Custom pullup	resetb	66 µA	250 µA

12 Defect Categorization

12.1 Introduction

Two distinct categories of defects are discussed in this section:

- pixel defects (*Section 12.2* - *Section 12.5*)
- physical aberrations (*Section 12.6*)

The two categories are differentiated in terms of test methodology as explained below. STMicroelectronics aim is to test our products to ensure that the end customer only receives the highest quality devices.

12.2 Pixel defects

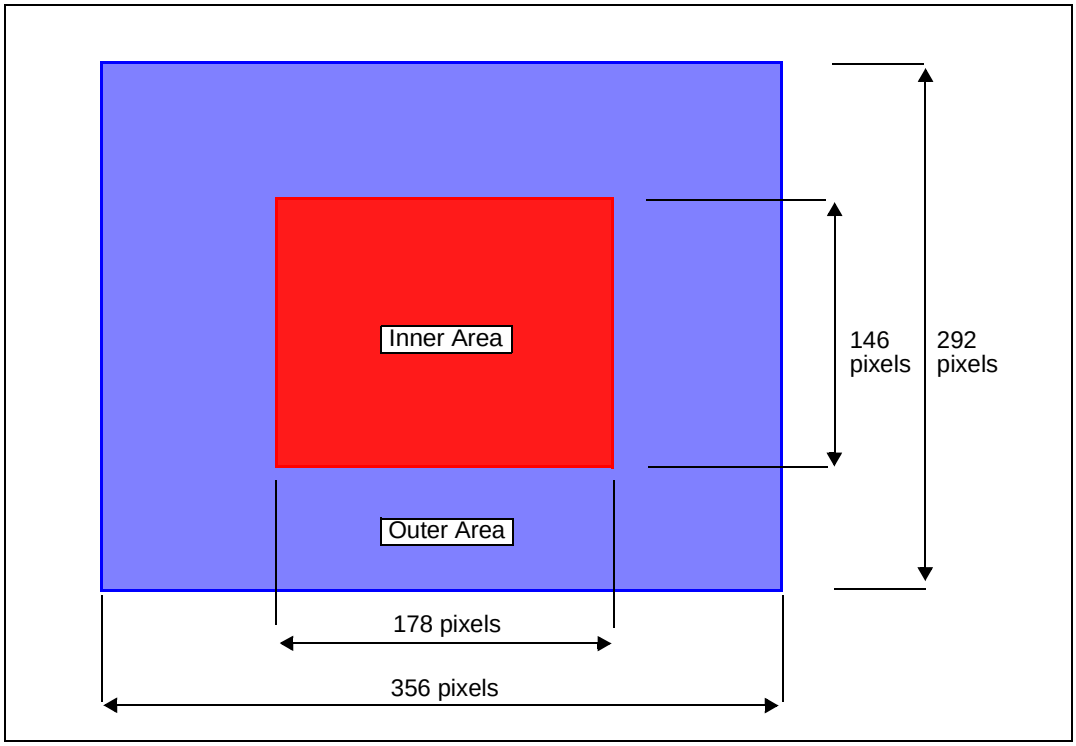
All packaged CMOS image sensors can contain impurities, either silicon faults, optical blemishes or external dirt particles which can be introduced in the product at various stages of the manufacturing process. These impurities can manifest themselves as pixel defects, that is a pixel whose output is not consistent with the level of incident light falling on the image sensor. Precise definitions of the type of pixel defects tested by STMicroelectronics are outlined below. The ability to identify and correct these defects is central to our products design requirements and the quality assurance, through test, of STMicroelectronics sensor products.

STMicroelectronics produces a number of hardware coprocessors and software drivers that implement defect correction algorithms. The defect correction algorithms ensure that the VV6411 sensor in conjunction with a companion STMicroelectronics coprocessor will produce a high quality final image.

12.3 Sensor array area definition

For specific aspects (refer to couplet test, see *Section 12.4.3*) of pixel defect testing, the image sensor array is subdivided into two regions as follows:

Figure 50: VV5411/VV6411 array



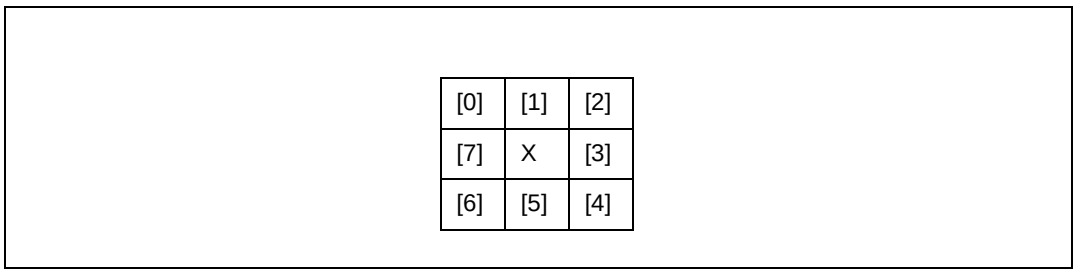
The inner array in *Figure 50* above is centre justified, in the x and y axis, with respect to the outer array. The inner array is 50% of the full width and 50% of the full height of the larger outer array, therefore the inner array is one quarter of the area of the outer array.

12.4 Pixel fault definitions

12.4.1 Pixel fault numbering convention

Please find the pixel notation described in *Figure 51* below. For test purposes, the 3x3 array describes 9 bayer pixels of a common color, i.e. pixels are Red, Green or Blue. The pixel under test is **X**.

Figure 51: Pixel numbering notation

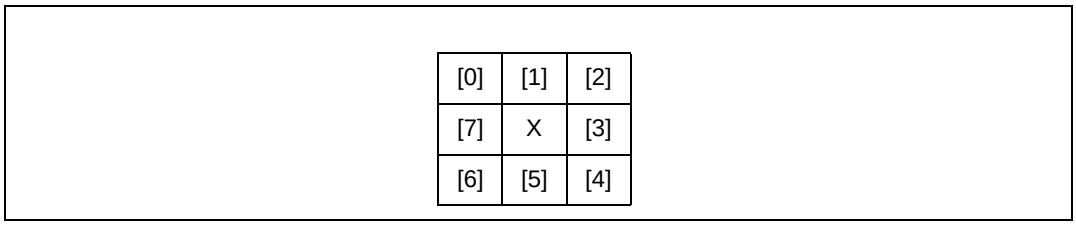


12.4.2 Single pixel faults

STMicroelectronics define a single pixel fail as a failing pixel with no failing adjacent neighbors of the same color. A single pixel fail can be a “stuck at white” where the output of the pixel is permanently saturated regardless of the level of incident light and exposure level, a “stuck at black” where the pixel output is zero regardless of the level of incident light and exposure level or simply a pixel that differs from its immediate neighbors by more than the test threshold, (i.e. differ by more than 6.0% from pixel average of color space neighbors).

In the example from *Figure 52*, we assume the pixel ‘X’ is a fail. This pixel is categorized as single pixel fail if the pixels at positions [0],[1],[2],[3],[4],[5],[6] and [7] are “good” pixels that pass final test. The implemented test program will pass a sensor with up to 120 single pixel faults. Defect correction algorithms correct the single pixel faults in the final image.

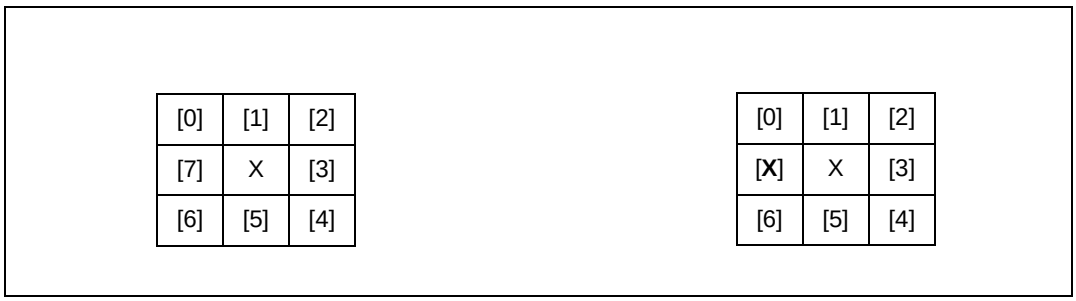
Figure 52: Single pixel fault



12.4.3 Couplet definition

A failing pixel at **X** with a failing pixel at position [0] or [1] or [2] or [3] or [4] or [5] or [6] or [7] so that there is a maximum of 2 failing pixels from the group of 9 pixels illustrated in *Figure 53* is described as a couplet fail. The example shown on the right in *Figure 53* has failing pixels at the centre location and at position [7].

Figure 53: General couplet examples



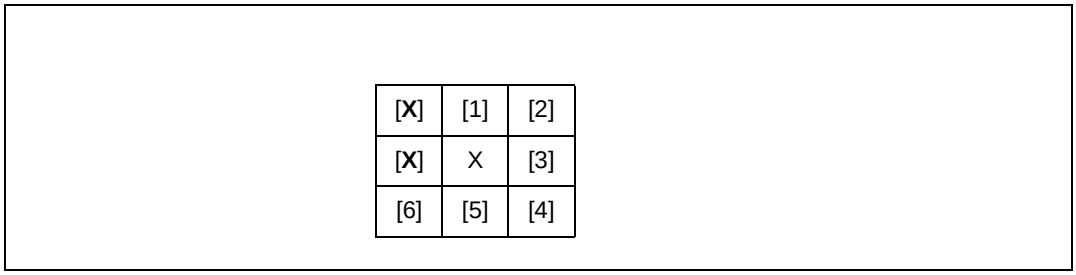
The basic couplet definition is further subdivided into minor and major couplets. With respect to the example in *Figure 53* a minor couplet is defined as a defect pixel pair where one pixel can be an extreme fail, that is a stuck at black or stuck at white, but the second pixel in the pair must differ from the convolved local pixel average by less than 15% of that average value. If the second pixel in the couplet differs by more than 15% of the local pixel average value then this would be defined as a major couplet.

It is important to note that the test program considers a couplet to comprise 2 independent pixels. If the test identifies two independent pixel fails (i.e. differ by more than 15% from pixel average of neighbors) that form a couplet with 2 minor pixel fails within the inner area then the device will fail the test and be rejected. If however, the test identifies 2 couplets where the pixels span the border between the inner and outer areas where only one of the pixels in the inner area is determined to be major and the other a minor fail then this device would pass the test.

12.4.4 Cluster definition

We define a cluster fail as a failing pixel with at least two neighboring failing pixels. In the example from *Figure 54* , there are additional pixel fails in positions [0] and [7]. This example constitutes a cluster. A sensor containing a cluster is always rejected.

Figure 54: Cluster example



12.5 Summary pass criteria

Table 68: Sensor pixel defect pass criteria

Single pixel fails	Minor Couplet[a]	Major Couplet[b]	Clusters
<=120	1 (2)	0	0

a. Test program will allow maximum of one minor couplet in inner zone of pixel array.
Test program will allow maximum of two minor couplets in outer zone of pixel array.

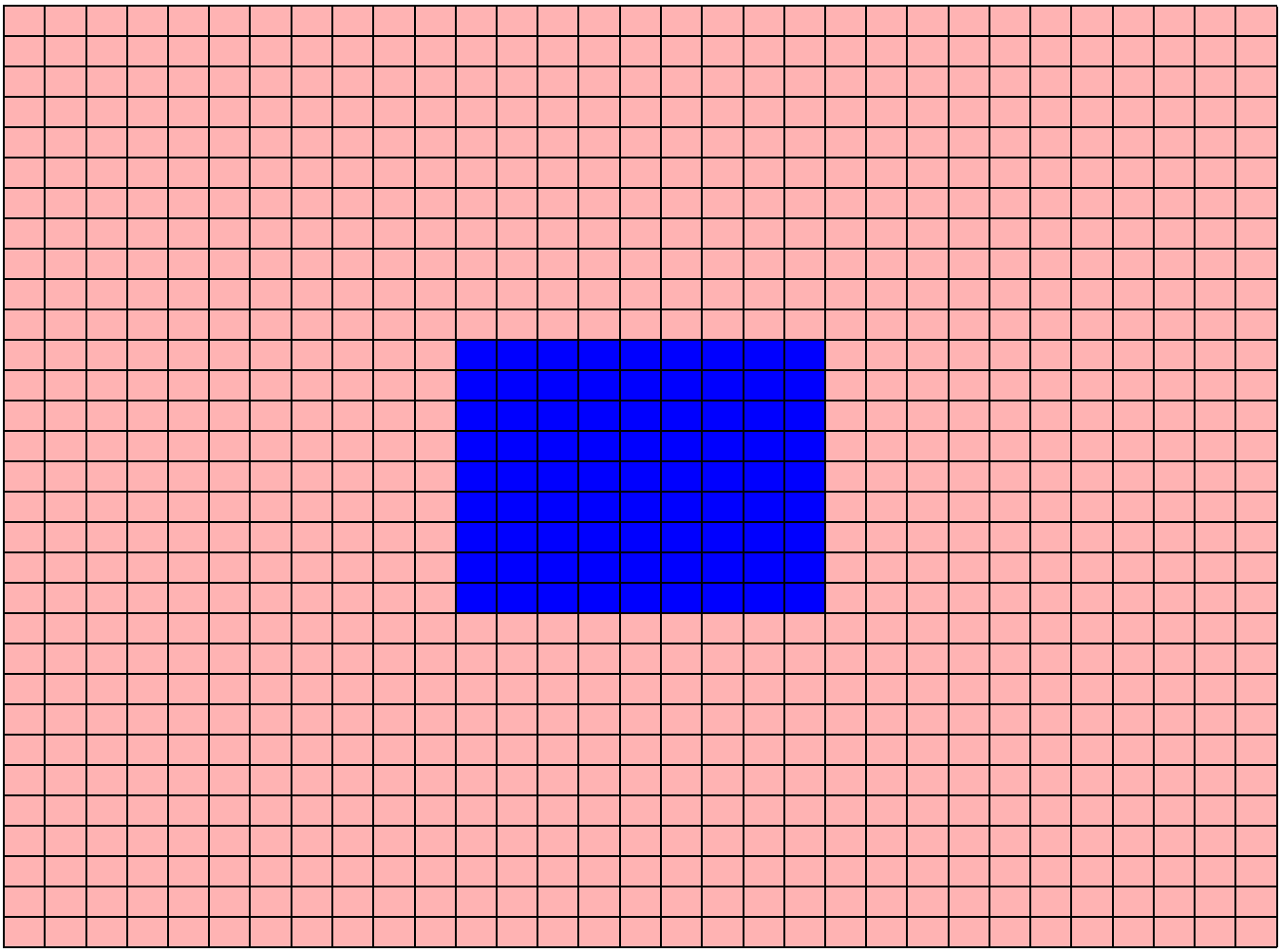
b. No major couplet allowed.

12.6 Physical aberrations

Silicon surface irregularities and external marks, both pits and deposits, on the package glass lids can cause the image quality deterioration. STMicroelectronics recognize that this could compromise product quality and therefore have introduced a specific test algorithm to identify and reject samples that display these phenomena. The pass/fail criteria for this test are given in *Section 12.6.1*.

12.6.1 Test details

Table 69: Test area definition



The test defines 2 regions:

- Small, 9 pixel by 9 pixel region with pixel under test at the centre of this region (shaded blue in *Table 69*)
- Larger, 31 pixel by 31 pixel region (shaded red in *Table 69*)

An average value is calculated for both the ‘small’ and ‘large’ regions.The regions then scan across the whole array in order to evaluate every pixel. Due to the nature of the test, it is only necessary to utilize the red pixels. The next stage of the test is the creation of a pixel map which will contain coordinates of the failing pixels. A pixel location is identified as a fail in the map if it satisfies the criteria outlined in *Table 70* below.

Table 70: Criteria for pixel to be entered in failure map

Pixel location is a fail in map if
(Small average < (Large average - (1.2% of Large average)) OR (Small average > (Large average + (1.2% of Large average))

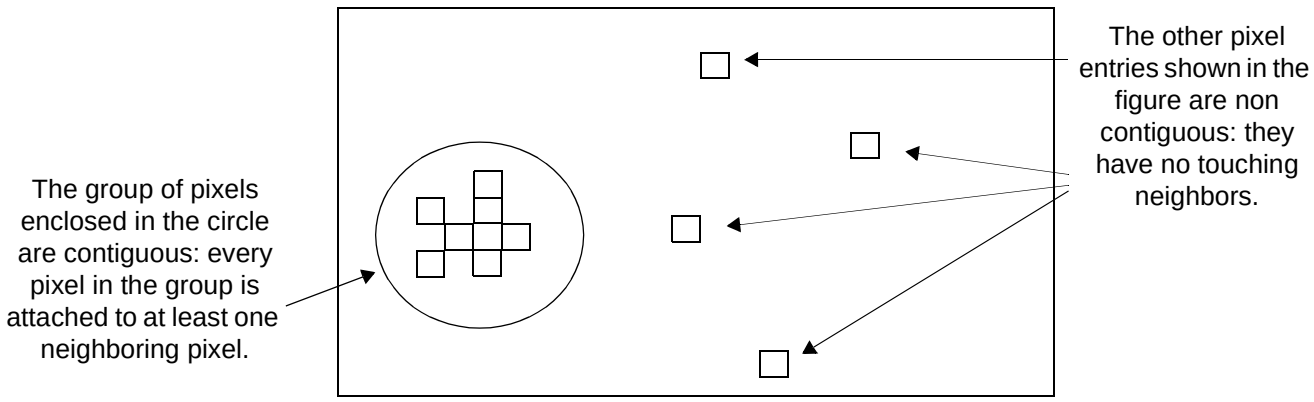
The contents of the fail map are then used to determine whether the sensor will fail the physical aberration test. The fail criteria are given in Table 71 below:

Table 71 : Physical aberration test fail criteria

Fail physical aberration test if
> 82 contiguous[a] pixel entries in the failure map

a. An example of contiguous pixels entries is given in *Figure 55* below

Figure 55: Contiguous pixels example



13 Pinouts and pin descriptions

13.1 36pin CLCC pin description

Figure 56: 36 pin CLCC package pin assignment

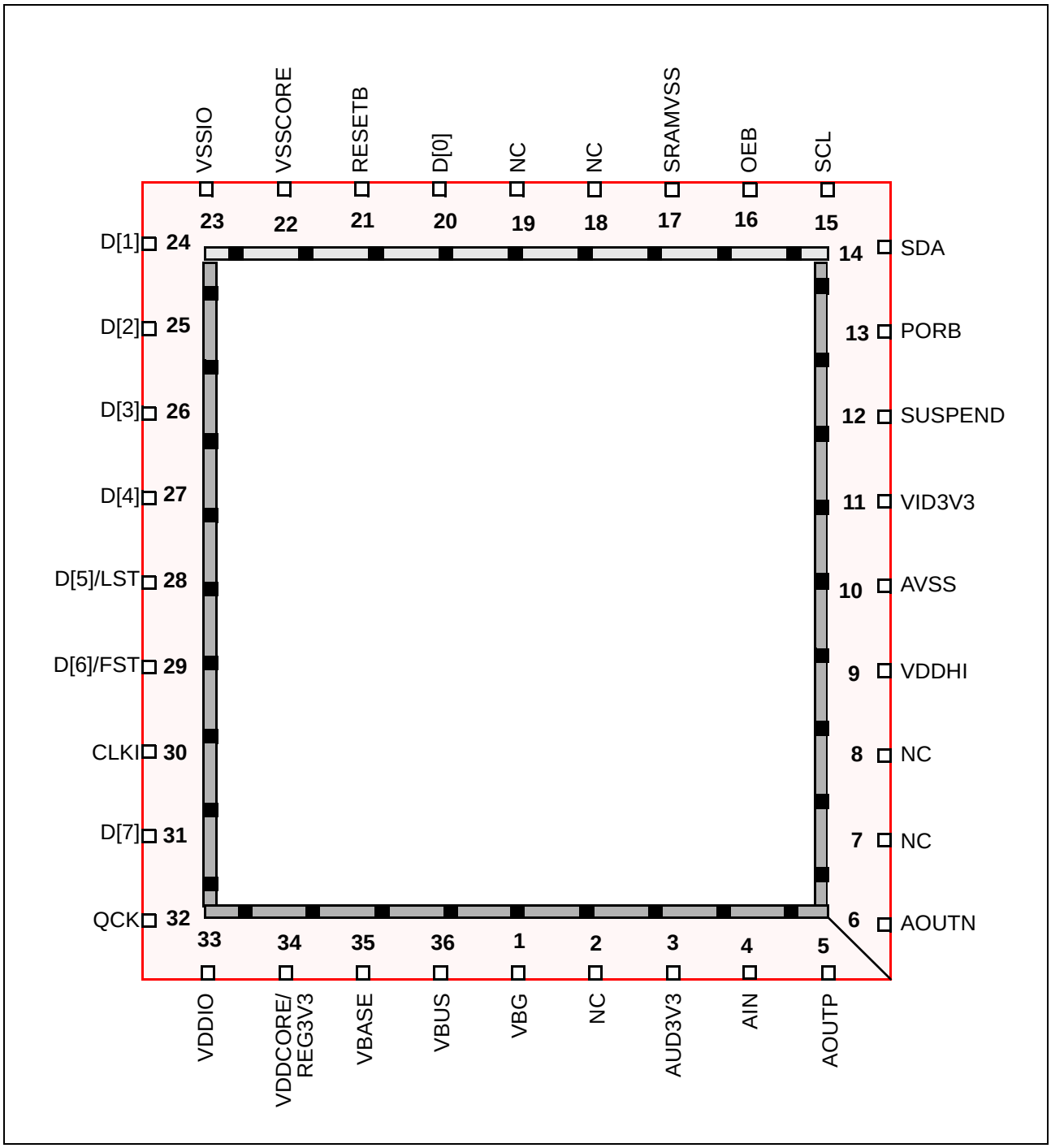


Table 72: 36 pin CLCC pin description

Name	Pin number	Type	Description
POWER SUPPLIES			
AVSS	10	GND	Core analog ground and reference supplies.
SRAMVSS	17	GND	In-column SRAM analog ground.
VDDcore/ Reg3V3	34	PWR	Digital logic power.
VDDio	33	PWR	Digital pad ring power.
VSScore	22	GND	Digital logic ground.
VSSio	23	GND	Digital pad ring ground.
Vid3V3	11	PWR	On-chip Video Supply Voltage Regulator Output
Aud3V3	3	PWR	On-chip Audio Amplifier Voltage Regulator Output
ANALOG SIGNALS			
VBG	1	OA	Internally generated bandgap reference voltage 1.22V
VDDHI	9	IA	Voltage doubler output, 4.6V -> 4.8V
VBase	35	OA	Drive for base of external bipolar
Vbus	36	IA	Incoming power supply 3.3 -> 6V
AIN	4	IA	Analog input to Audio Amplifier
AOutP	5	OA	Analog output of Audio Amplifier (positive)
AOutN	6	OA	Analog output of Audio Amplifier (negative)
PORB	13	OD	Power-on Reset (Bar) Output.
DIGITAL VIDEO INTERFACE			
D[4 D[3] D[2] D[1] D[0]	27 26 25 24 20	ODT	Tri-stateable 5-wire output data bus. - D[4] is the most significant bit. - D[4:0] have programmable drive strengths 2, 4 and 6 mA
QCK	32	ODT	Tri-stateable data qualification clock.
LST/D[5]	28	ODT	Tri-stateable Line start output May be configured as tri-stateable output data bit 5 D[5].
FST/D[6]	29	ODT	Tri-stateable Frame start signal. May be configured as tri-stateable output data bit 6 D[6].
D[7]	31	ODT	Tri-stateable Data wire (ms data bit). May be configured as tri-stateable output data bit 6 D[6].
OEB	16	ID↓	Digital output (tri-state) enable.
DIGITAL CONTROL SIGNALS			
RESETB	21	ID↑	System Reset. Active Low. May be configured as System Sync. Active Low.

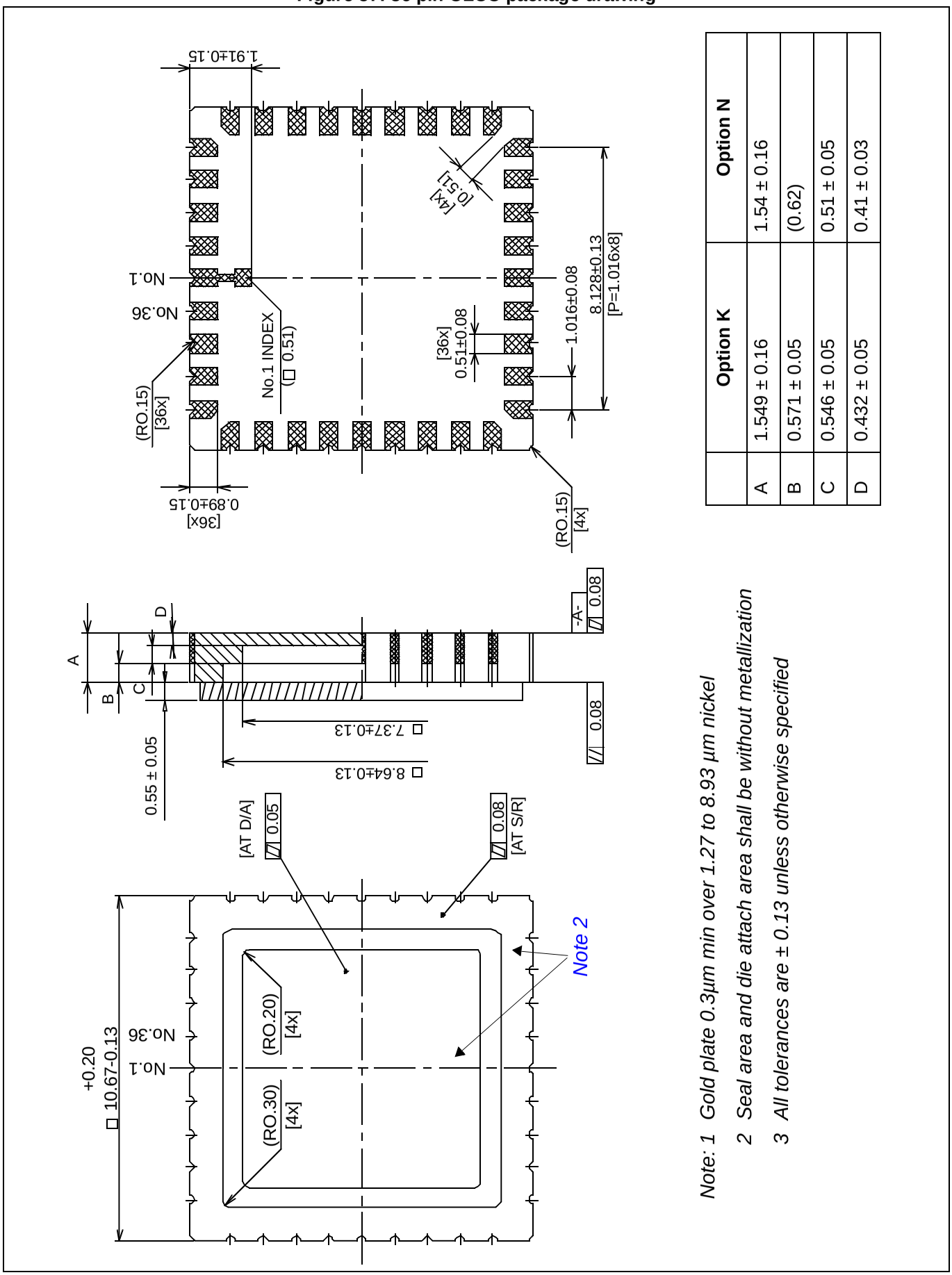
Table 72: 36 pin CLCC pin description

Name	Pin number	Type	Description
SUSPEND	12	ID↑	USB Suspend Mode Control signal. Active High. If this feature is not required then the support circuit must pull the pin to ground. The combination of an active high signal and pull up pad was chosen to limit current drawn by the device while in suspend mode.
I^2C			
SCL	15	BI↑	Serial bus clock (input only).
SDA	14	BI↑	Serial bus data (bidirectional, open drain).
SYSTEM CLOCKS			
CLKI	30	ID↓	Schmitt Buffered Clock input or LVDS positive Clock input
NOT CONNECTED			
NC	2, 7, 8, 18, 19		Not connected

Key			
A	Analog Input	D	Digital Input
OA	Analog Output	ID↑	Digital input with internal pull-up
BI	Bidirectional	ID↓	Digital input with internal pull-down
BI↑	Bidirectional with internal pull-up	OD	Digital Output
BI↓	Bidirectional with internal pull-down	ODT	Tri-stateable Digital Output

14 Package Details

Figure 57: 36 pin CLCC package drawing



	Option K	Option N
A	1.549 ± 0.16	1.54 ± 0.16
B	0.571 ± 0.05	(0.62)
C	0.546 ± 0.05	0.51 ± 0.05
D	0.432 ± 0.05	0.41 ± 0.03

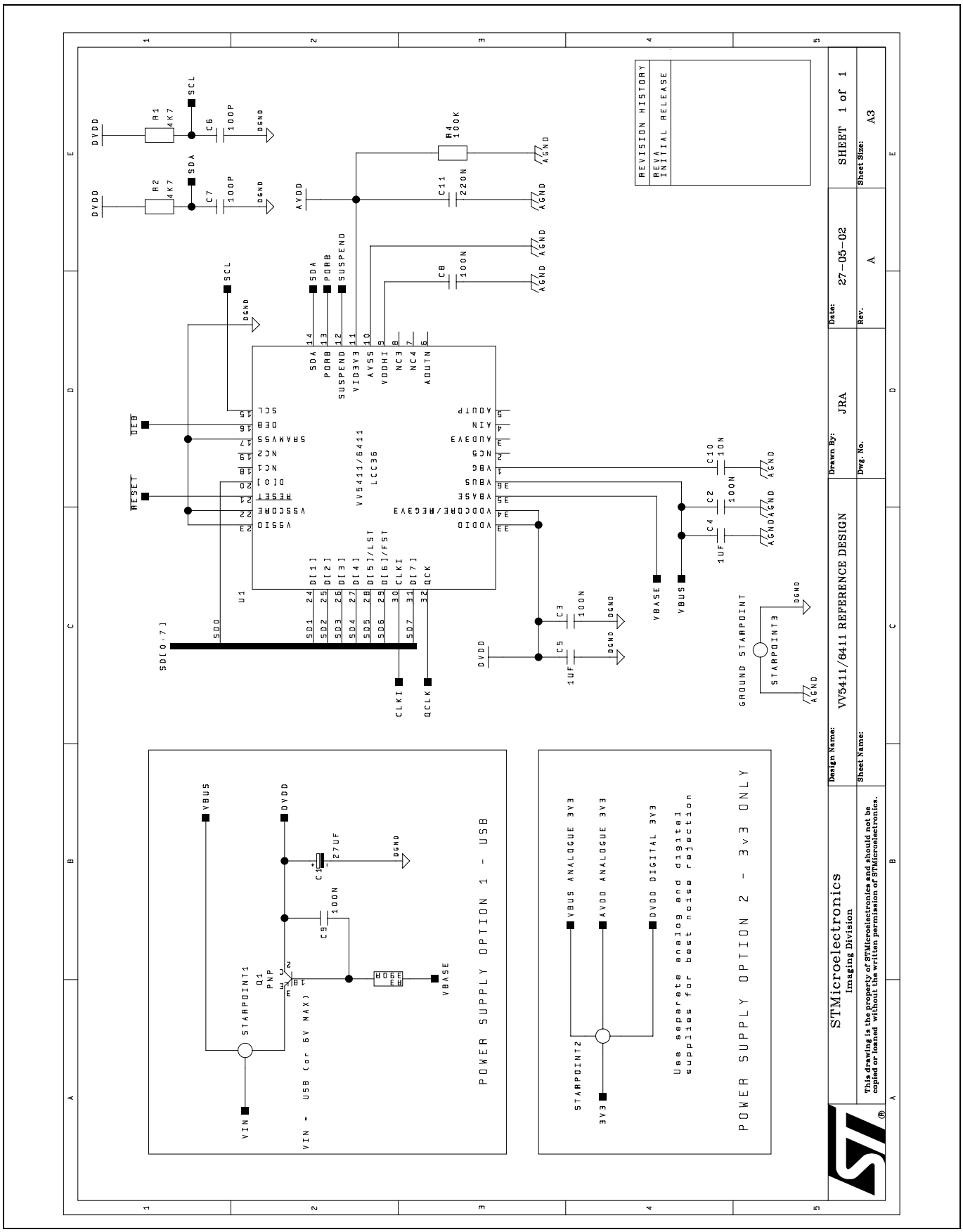
Note: 1 Gold plate 0.3µm min over 1.27 to 8.93 µm nickel

2 Seal area and die attach area shall be without metallization

3 All tolerances are ± 0.13 unless otherwise specified

15 Recommended VV5411/6411 support circuits

15.1 Support circuit for 36-pin CLCC option



16 Evaluation kits (EVK's)

It is highly recommended that an Evaluation Kit (EVK) is used for initial evaluation and design-in of the VV5411/6411. A VV5411/VV6411 evaluation kit can now be ordered. Please contact STMicroelectronics for details.

It is important to note that the 8 wire output mode is not supported by the evaluation kits. The 4 wire and 5 wire modes are fully supported by the evaluation kits.

17 Ordering details

Table 73: VV6411/VV5411 ordering details

Part Number	Description
VV5411C036	36pin CLCC packaged CIF monochrome sensor
VV6411C036	36pin CLCC packaged, microlensed CIF ColorMOS sensor
STV-EVK-E02	Evaluation kit for VV5411
STV-EVK-E01	Evaluation kit for VV6411