ST-NXP Wireless

STW4511

7-channel power management unit

Preliminary Data

Features

2 step-down converters

- Vsdc1: 1 V to 1.5 V
  - 600 mA maximum output current
  - I2C control possibility
  - programmable default output voltage (1.4 V predefined value[a])
  - OFF mode on external Pwren signal
- Vsdc2: 1.8 V
  - 600 mA maximum output current
  - OFF mode on external Pwren signal

5 low-drop output regulators

- Vdig: 1.0 V (100 mA) to 1.5 V - 250 mA max
  - Match up Vsdc1 output voltage
  - Always switched on after start-up (even on reset)
- Vana1: 1.8 V - 150 mA max
  - Match up Vsdc2 output voltage
  - Always switched on after start-up (even on reset)
- Vana2/3/4: 1.8, 2.5, 2.8, 3.3 V - 150 mA max
  - ON or OFF mode possibility at start-up
  - ON/OFF mode controlled by I2C or by Pwren = 0 (except for Vana3 only controlled by Pwren =0)

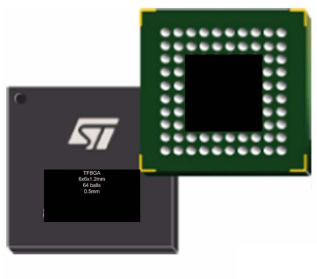
Battery supervisor

- Programmable minimum battery level

Power supply switches

- 2 internal switches for external DRAM memory supply (1.8 V)

a. This value can be one of the available output voltages (see Power Control Register @ 05h) - Please contact ST-NXP Wireless sales if different predefined output voltage is needed.



TFGA, 64 balls, 6 mm x 6 mm x 1.2 mm with 0.5mm pitch

- Supply via Vana1 in low power mode
- Supply via Vsdc2 in high power mode

Miscellaneous

- I2C control
- Temperature shutdown
- Internal clock generation for supply switching and state machine sequencing

Application

- Portable navigation device (GPS)
- Portable multimedia player
- Personal digital assistant (PDA)
- Portable consumer equipment or handheld devices

Description

STW4511 is a 7-channel power management device developed for applications powered by one Li-Ion or Li-Polymer cell. STW4511 embeds 2 highly efficient step-down DC/DC converters and 5 LDO regulators. STW4511 enables two always-on LDOs for low system quiescent current. Integrated switches are used to keep the DRAM memories supplied even in stand by mode.

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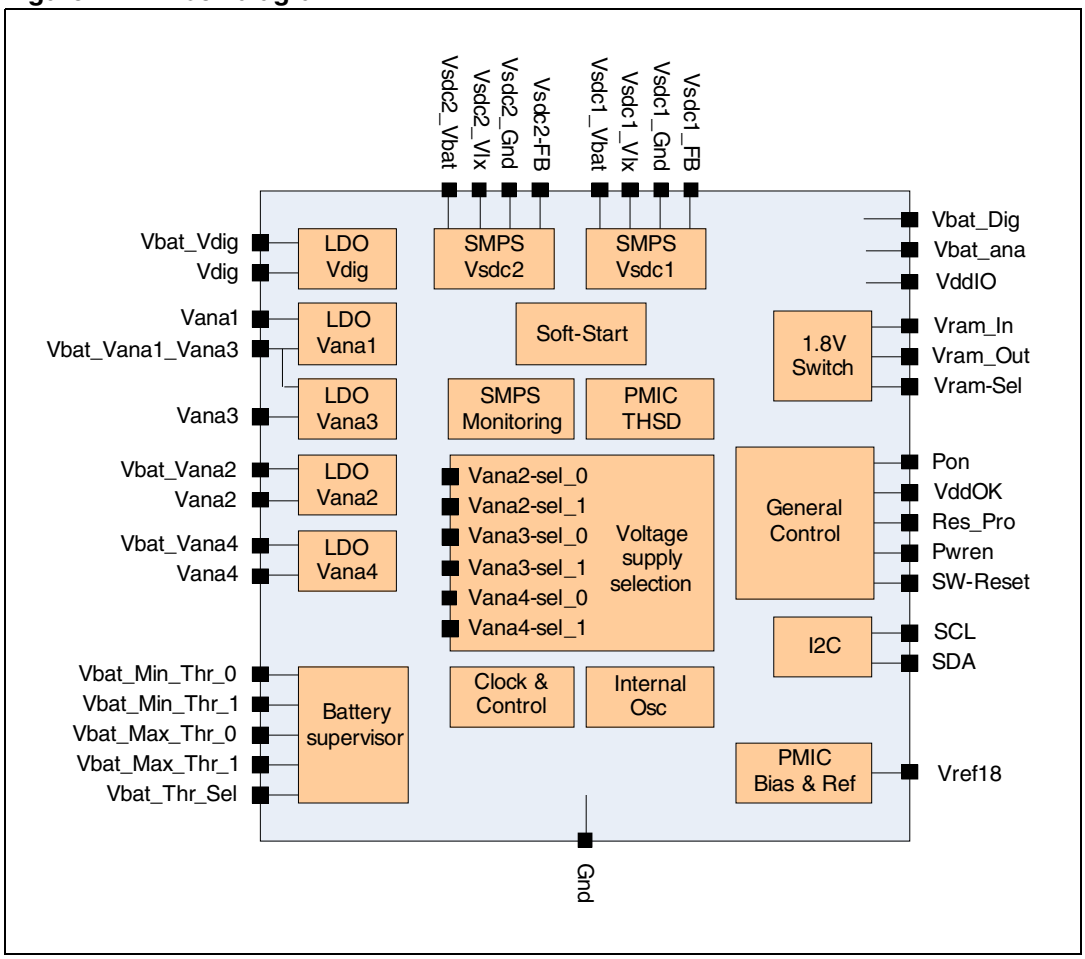
1 Product overview

The STW4511 device is a power management unit (PMU) that integrates:

- two step down converters,
- five LDOs, among which two are always switched on,
- RAM supply in low power mode,
- autonomous state machine handling smooth supply sequencing,
- die temperature shutdown,
- battery supervisor with programmable minimum battery voltage and processor reset.

1.1 Block diagram

Figure 1. Block diagram



1.2 Ball information

1.2.1 Package ball map

Table 1. Package ball out for TFBGA 64 - 6 mm x 6 mm with 0.5 mm pitch

	1	2	3	4	5	6	7	8	9	10
A	Reserved	Vsdc2_Gnd	Vsdc2_Vlx	Vsdc2_Vbat	Gnd_ana	Vdig	Vana1	Vbat_ Vana1_ Vana3	Vana3	Vref18
B	Reserved	Vsdc2_Gnd	Vsdc2_Vlx	Vsdc2_Vbat	Vsdc2_FB	Vbat_ana	Vbat_Vdig	Not used	Reserved	Pon
C	Gnd_Dig	Reserved							Reserved	Vsdc1_FB
D	Vbat_dig	Reserved							Vsdc1_Gnd	Vsdc1_Gnd
E	Vram_In	Reserved							Vsdc1_Vlx	Vsdc1_Vlx
F	Vram_Out	Reserved							Vsdc1_Vbat	Vsdc1_Vbat
G	Vram_Sel	Vana4_ Sel_0							Vbat_Min_ Thr_0	Vana2
H	VddOK	Not used							Not used	Vbat- Vana2
J	Res_Pro	Not used	Not used	Vana4_ Sel_1	Pwren	Vana2_ Sel_0	Vana3_ Sel_0	Vbat_Max_ Thr_0	Not used	VddIo
K	SW_Reset	Vbat_ Vana4	Vana4	SCL	SDA	Vbat_Thr_ Sel	Vana2_ Sel_1	Vana3_ Sel_1	Vbat_Max_ Thr_1	Vbat_Min_ Thr_1

1.2.2 Ball description

The device includes four ball types:

- VddD/VddA: digital/analog positive supply
- GndD/GndA: digital/analog ground
- DO/DI/DIO: digital output/input/input-output
- AO/AI/AIO: analog output/input/input-output

Table 2. Ball description

Ball number	Name	Type	Description
Step-down converters			
F9, F10	Vsdc1_ Vbat	VddA	SMPS dedicated supply input
E9, E10	Vsdc1_Vlx	AO	SMPS coil output
C10	Vsdc1_FB	AI	SMPS feedback
D9, D10	Vsdc1_Gnd	GndA	SMPS dedicated ground
A4, B4	Vsdc2_ Vbat	VddA	SMPS dedicated supply input
A3, B3	Vsdc2_Vlx	AO	SMPS coil output
B5	Vsdc2_FB	AI	SMPS feedback
A2, B2	Vsdc2_Gnd	GndA	SMPS dedicated ground
14	Switched converters total ball number		

Table 2. Ball description (continued)

Ball number	Name	Type	Description
LDO converters			
A8	Vbat_Vana1_Vana3	VddA	LDO dedicated supply input
A7	Vana1	AO	LDO output
H10	Vbat_Vana2	VddA	LDO dedicated supply input
G10	Vana2	AO	LDO output
A9	Vana3	AO	LDO output
B7	Vbat_Vdig	VddA	LDO dedicated supply input
A6	Vdig	AO	LDO output
K2	Vbat_Vana4	VddA	LDO dedicated supply input
K3	Vana4	AO	LDO output
9	Linear converter total ball number		
I2C interface			
K5	SDA	DI/O (1.8V)	I2C data interface
K4	SCL	DI (1.8V)	I2C clock interface
2	Control interface ball number		
General control for power supplies			
B10	Pon	DI (Nmos) pull-down 1.5 MΩ	Power on of the supplies part
H1	VddOK	DO (1.8V)	SMPS high value monitoring status
J1	Res_pro	DO (1.8V)	Processor reset
J5	Pwren	DI (1.8V) pull-up 1.5MΩ	Sleep high power mode/low power mode control
K1	SW_reset	DI (1.8V) pull-up 1.5MΩ	S/W reset from processor
5	PMIC general control total ball number		
Selection voltage inputs			
J6	Vana2-Sel_0	DI (Vbat)	Voltage selection
K7	Vana2_Sel_1	DI (Vbat)	Voltage selection
J7	Vana3_Sel_0	DI (Vbat)	Voltage selection
K8	Vana3_Sel_1	DI (Vbat)	Voltage selection
G2	Vana4_Sel_0	DI (Vbat)	Voltage selection
J4	Vana4_Sel_1	DI (Vbat)	Voltage selection
G9	Vbat_Min_Thr_0	DI (Vbat)	Battery voltage threshold to set the processor in reset

Table 2. Ball description (continued)

Ball number	Name	Type	Description
K10	Vbat_Min_Thr_1	DI (Vbat)	Battery voltage threshold to set the processor in reset
J8	Vbat_Max_Thr_0	DI (Vbat)	Battery voltage threshold to set the processor in HPM
K9	Vbat_Max_Thr_1	DI (Vbat)	Battery voltage threshold to set the processor in HPM
10	Total voltage selection inputs		
Other inputs and outputs			
A10	Vref18	AO	Internal reference of the power management device
J10	VddIO	DI	IO power supply
B6	Vbat-ana	VddA	PM analog part supply
D1	Vbat-Dig	VddD	Oscillator part supply
K6	Vbat_Thr_Sel	DI (Vbat)	Battery voltage supervision enable
C1	Gnd_Dig	GndD	Ground
A5	Gnd_Ana	GnDA	Ground
E1	Vram_In	AI	1.8V switch input from Vsdc2 for memory
F1	Vram_Out	AO	1.8V output
G1	Vram_sel	DI (Vbat)	Memory supply switch enable.
D2	Reserved	Opened	Test purpose
E2	Reserved	Opened	Test purpose
F2	Reserved	Opened	Test purpose
B9	Reserved	Opened	Test purpose
A1	Reserved	GndA	Test purpose
B1	Reserved	GndA	Test purpose
C2	Reserved	GndA	Test purpose
C9	Reserved	GndA	Test purpose
16	Other I/O ball number		
Not used balls			
B8, H2, J2, J3, H9, J9	Not used	Opened	
6	Not used		
64	Overall ball number		

2 STW4511 description

2.1 Introduction

The device integrates power supplies for the processor and associated peripherals.

2.2 Power on

The device is in power on mode when Pon is set to 1 (Pon = 1). Power on state is also reached by connecting directly the input pin to Vbat or to a voltage above 1 V.

When Pon equals 0 (Pon = 0) the device completely shuts down. Thus, it is possible to make a full hard reset of the supplies.

2.3 High power mode (HPM)

The device is in high power mode (HPM) when Pwren is set to 1 (Pwren = 1). The converter outputs are then regulated and able to supply the dedicated application features.

At power on the device must be in high power mode. For that purpose, the IC includes an internal pull-up on the Pwren ball.

2.4 Low power mode (LPM) or sleep mode

The device is in sleep mode when Pwren is set to 0 (Pwren = 0).

Vana1 and Vdig signal values do not change.

The two step-down converters are switched OFF. The overall consumption is then reduced to leakage current.

Vana2, Vana3, and Vana4 are switched off if Vana2_Vana3_Off = 1 and Vana4_Off = 1 (see *Power control register @ 09h*). In other cases, Vana2, Vana3, and Vana4 remain in high power mode.

2.5 Battery supervisor

STW4511 has two different battery voltage thresholds:

- battery voltage falling threshold:
  when the battery voltage drops down below this threshold, the device shuts down
- battery voltage rising threshold:
  when the battery voltage rises above this threshold, the device can (re-)start in high-power mode if Pon is set to 1 (Pon=1).

The battery supervisor feature is enabled when Vbat_Thr_Sel ball is set to 1 (Vbat_Thr_Sel = 1). Low threshold values stop the device when the battery is very low.

The battery supervisor falling/rising thresholds are programmable via dedicated signals, **Vbat_Min_Thr_0/1** and **Vbat_Max_Thr_0/1** respectively. These pins can be connected either to the battery voltage or to ground.

Table 3. Battery voltage falling threshold

Vbat_Min_Thr0	Vbat_Min_Thr1	Vbat-Thr-En	Threshold value (V)
0	0	1	2.7
0	1	1	2.85
1	0	1	3.05
1	1	1	3.3
X	X	0	2.25

Table 4. Battery voltage rising threshold

Vbat_Max_Thr0	Vbat_Max_Thr1	Vbat-Thr-En	Threshold value (V)
0	0	1	3.4
0	1	1	3.5
1	0	1	3.6
1	1	1	3.7
X	X	0	2.65

The rising threshold ensures that the battery has enough energy to supply the whole application at start up. The device starts when the battery supply rises above the threshold rising value.

Below the falling down threshold the battery has not enough energy to supply the always-on parts, the device is completely switched off.

2.6 RAM memory supply

2.6.1 1.8V switch definition

STW4511 includes integrated switches that supply the DRAM memory

- with 1.8 V always-on supply in low power mode and,
- with 1.8 V supply from the step-down converter in high power mode.

The Vram_Out ball supplies the DRAM memory.

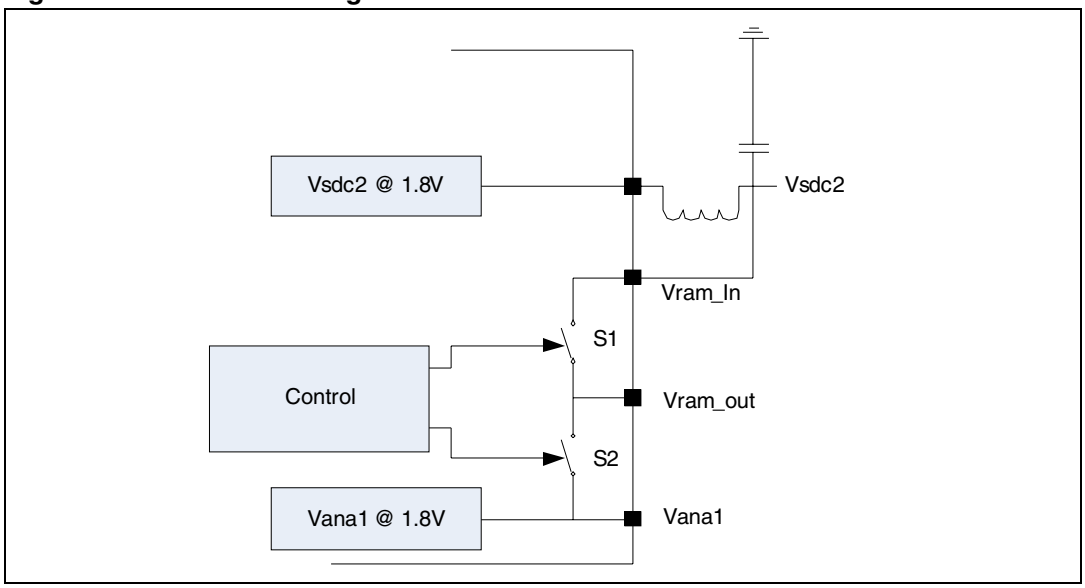
The Vram_Sel connected to the battery voltage enables the RAM memory supply. Vram_Sel is active high.

Vsdc2 output is connected to the Vram_In ball. An internal switch connects this input to the Vram_Out. This switch is closed only in high power mode.

An internal switch connects the Vana1 output (internal connection, no ball used) to the Vram_Out. This switch is closed only in low power mode, when PWREN signal is low.

When Pon is low, the Vram_Out is switched to ground via the use of a third internal switch.

Figure 2. 1.8V switch diagram



2.6.2 1.8 V switch electrical characteristics

Table 5. Electrical characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Vram input voltage		-3%	1.8	+3%	V
Vram output voltage		1.70	1.8	+3%	V
S1_I_max	Maximum current through the switch in HPM	140			mA
S2_I_max	Maximum current through the switch in LPM	0.3			mA
S1 Ron	Voltage = 1.8V		0.2		Ω
S2 Ron	Voltage = 1.8V @ Vbat=3.6V		0.08	1	kΩ

2.7 Control pin description

Control pin Pon

Pon input signal is active high. Pon signal is used to turn on the device and start the internal state machine that handles the supply sequencing.

Pon ball can be directly connected to the battery voltage.

Pon voltage must always be lower or equal to Vbat.

Control pin Pwren

Pwren input signal is active high. Pwren signal sets the device in high power mode.

At start up the Pwren signal is masked until the internal oscillator stabilizes and the device is biased. After this period, Pwren is handled by the device internal state machine.

When Pwren = 0 (low power mode):

- Vsdc1 and Vsdc2 are switched off
- Vana1 and Vdig remain in HPM
- Vana2/3/4 are switched off, but can remain in HPM (*Power control register @ 09h* - Vana2/3_OFF and Vana4_OFF)

When Pwren is not driven by external components (typically at start-up), an internal pull-up ties Pwren to high level to ensure power on in high power mode.

Control pin Res_pro

Res_pro is an output signal used to reset the processor. Res_pro is active low.

Res_pro = 0 when:

- the device is starting up,
- when the battery voltage drops below the battery voltage threshold programmed by the battery supervisor

Control pin VddOK

VddOK is an output signal pin active high. VddOK confirms that Vsdc1, Vsdc2 values are within the output voltage range.

VddOK falls to 0 when:

- Pwren = 0
- Vsdc1 or Vsdc2 values are below the defined threshold (output voltage monitoring), see *Table 15* in *Chapter 3: Electrical characteristics*.
- the battery voltage drops below the battery voltage threshold programmed by the battery supervisor

Control pin SW-reset

This input signal is used to reset all registers except the ones at 1Eh and 1Fh addresses. SW-reset signal is active low.

2.8 Power supply timing diagrams

Start up sequence

When Pon = 1

- Vana1 and Vdig are switched on, these LDO remain on until they are reset by Pon = 0.

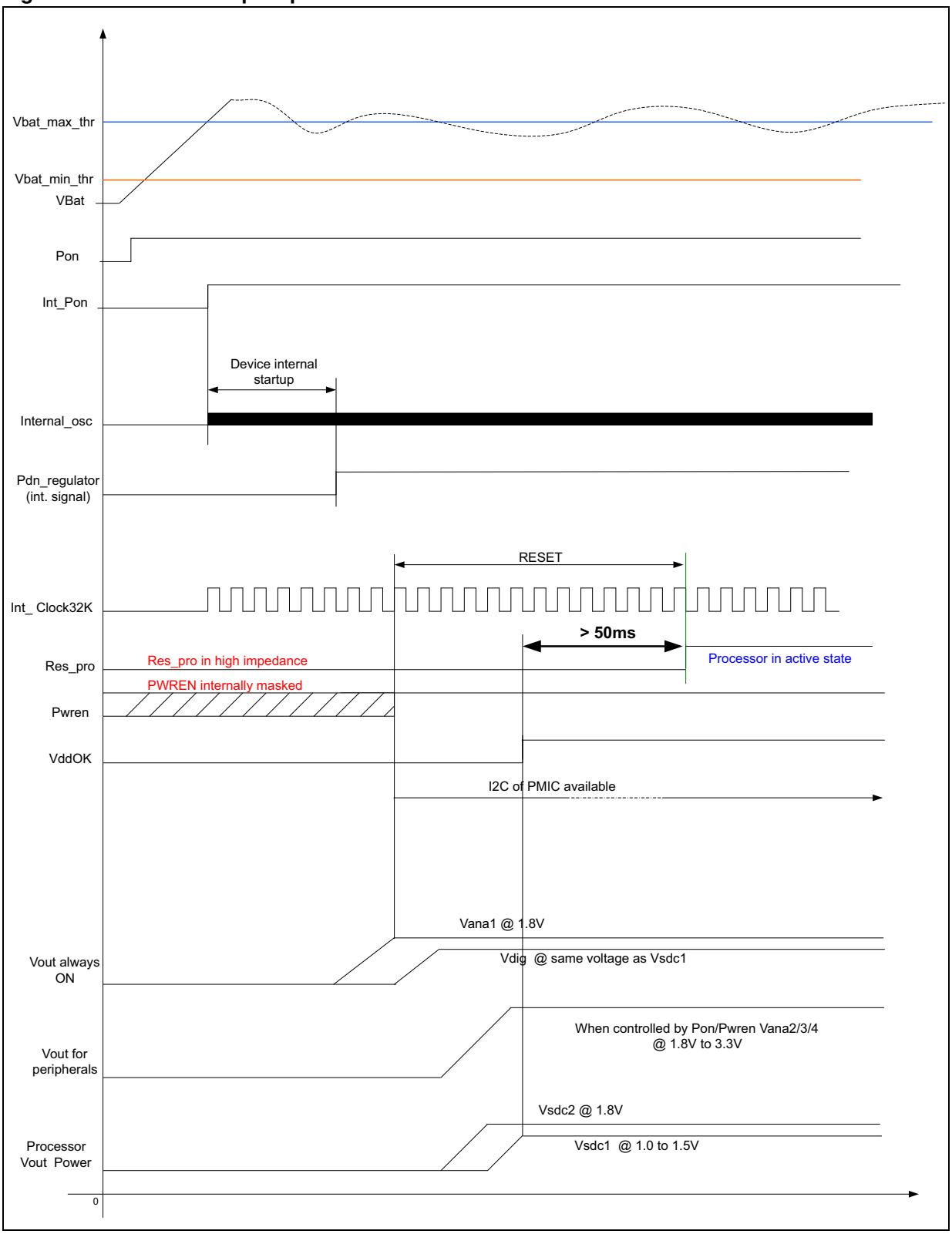
When Pon = 1 and Pwren = 1

- Vsdc2 and Vsdc1 are switched on only if vana1 and Vdig have also been switched on,
- Vana2, Vana3, Vana4 can start up simultaneously to supply the peripherals. Alternatively, Vana2, Vana3, Vana4 can be off at start up and then controlled by I2C (*Power control register @ 07h* - En_Vana4 and 08h - En_Vana2)
- Vana3 is switched on at the same time as Vsdc2.

When Res_pro = 1

- the processor is out of reset mode and the application is running.

Figure 3. Initial start up sequence

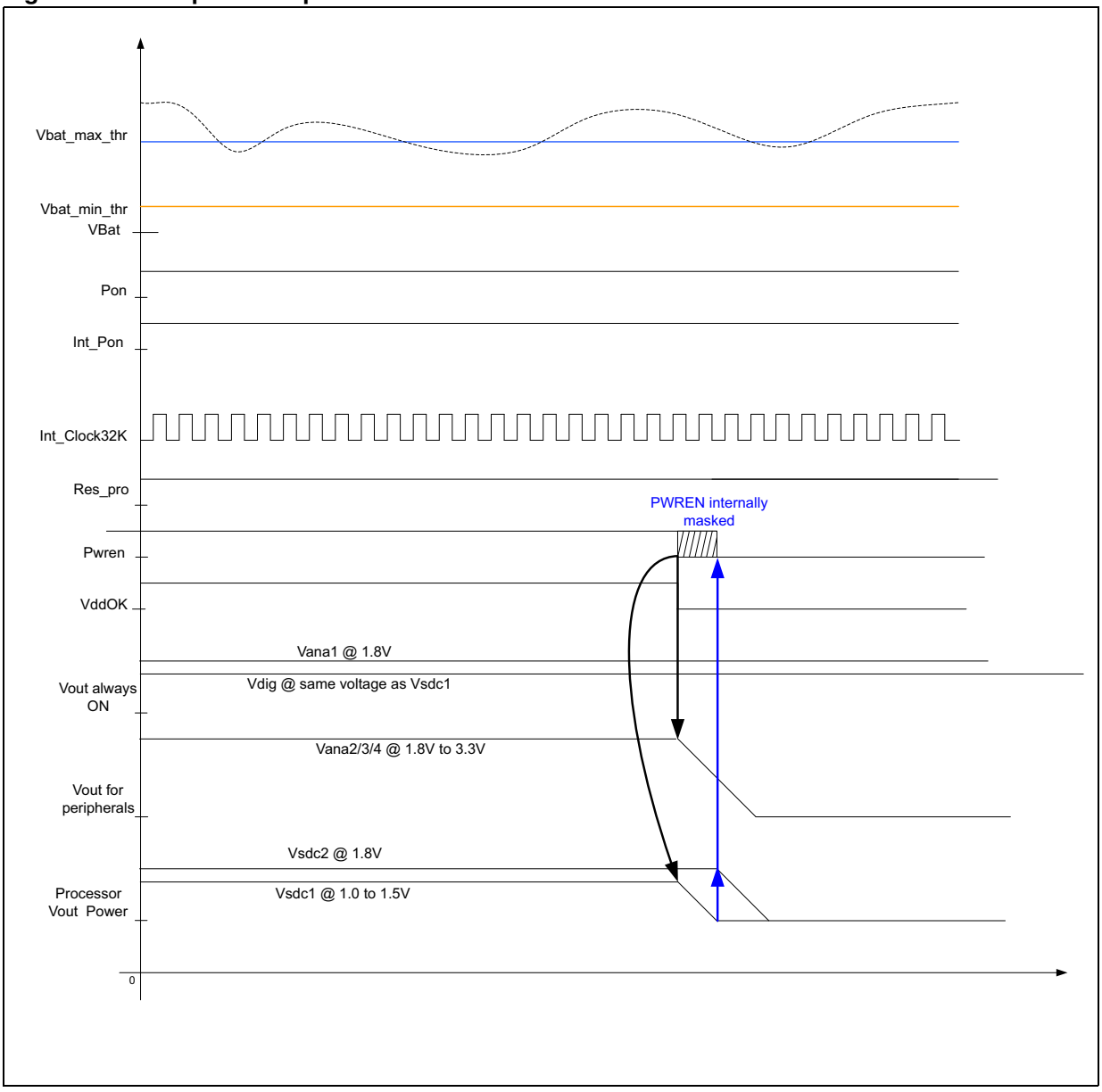


LPM mode sequence

When Pwren = 0

- Vsdc1 and Vsdc2 are switched off
- Vana1 and Vdig remain in HPM
- Vana2/3/4 can be in off mode or stay in HPM (*Power control register @ 09h* - Vana2/3_OFF, Vana4_OFF)

Figure 4. Low power sequence

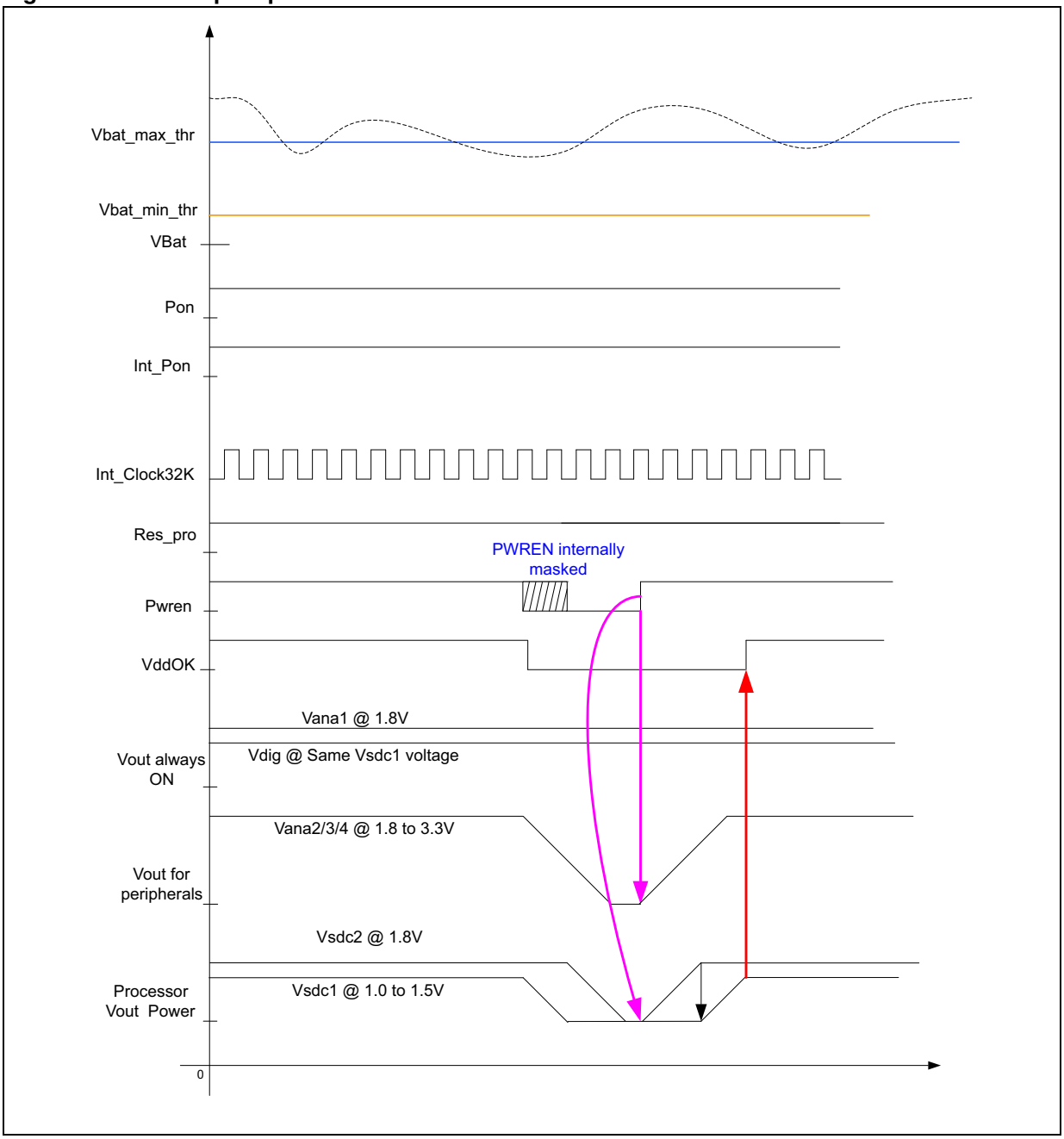


Wake-up sequence

The wake-up sequence occurs when Pwren goes from 0 to 1:

- Vana1 and Vdig stay in HPM
- Vsdc2 and Vsdc1 are switched on
- Vana2/3/4 are switched off or stay in HPM (*Power control register @ 09h* - Vana2/3_OFF, Vana4_OFF).

Figure 5. Wake-up sequence

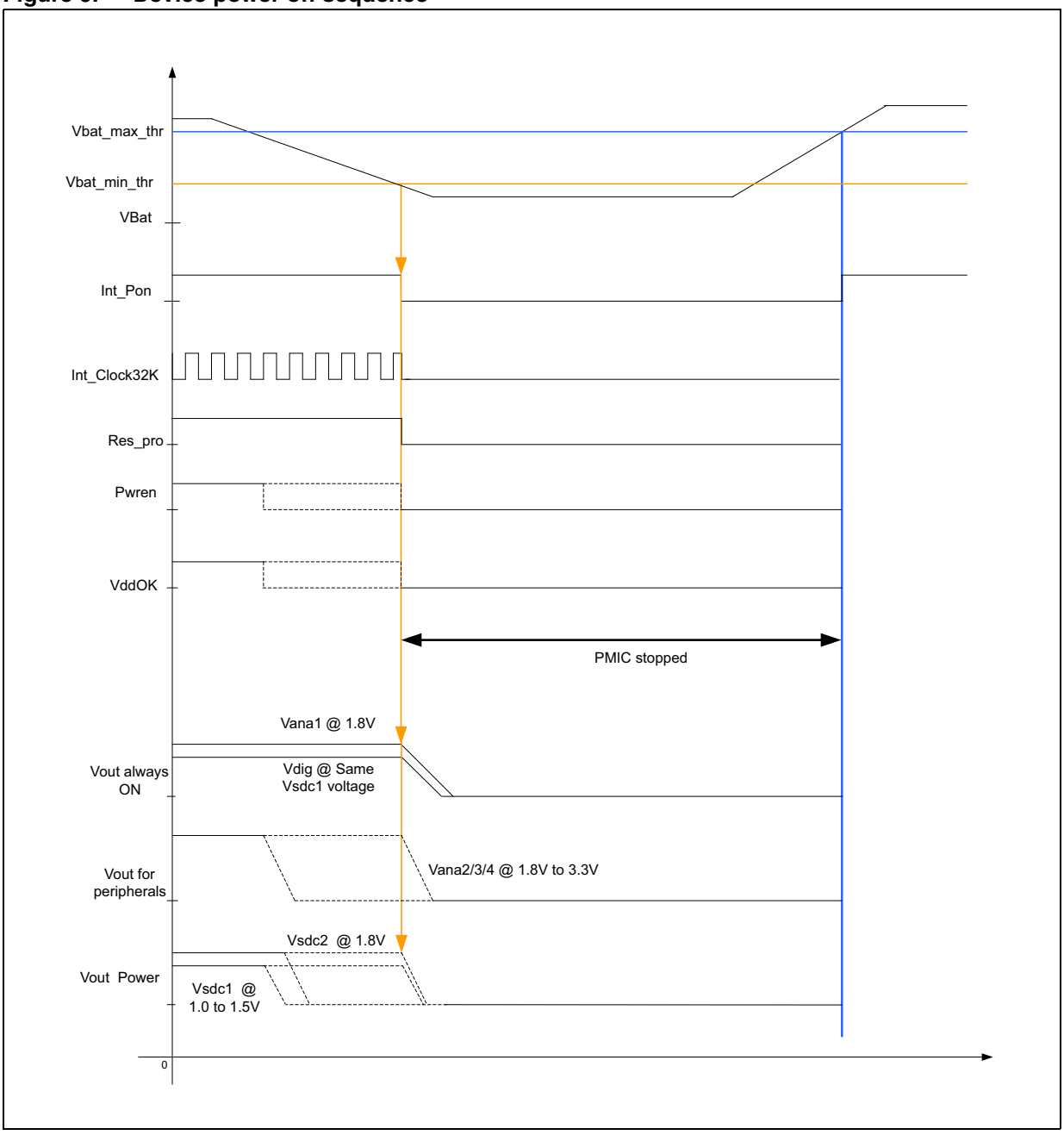


Device power-off sequence

The device power-off sequence occurs when the battery voltage falls under the Vbat-min-thr battery voltage threshold:

- all power supplies are turned off,
- a S/W threshold can be added to switch off the DC/DC converter before the low battery threshold is reached. This is a smart way to keep only the always-on LDO and let the processor in sleep mode. The application quickly restarts when an external power supply is plugged.

Figure 6. Device power off sequence



2.9 Power supplies

The device has 2 step-down converters and 5 LDO supplies.

2.9.1 Step-down converters

Vsdc1 DC/DC converter supply voltage

Vsdc1 is a step-down converter with a very high efficiency.

Adjustable voltage levels enable a dynamic scaling voltage suitable for any supply voltage with CMOS process.

Vsdc1 has 2 modes:

- high power mode (HPM) to supply the application
- low power mode (LPM) to switch off the output voltage.

The regulated output voltage levels are adjustable by controlling the dedicated registers via I2C interface (*Power control register @ 05h*). The output voltage has predefined values at start-up which can be chosen in the available range defined in the Power Control Register @ 05h (see *Note 1*).

The output voltage is coupled with the LDO Vdig to ensure the same output voltage values at both outputs.

The power supply is switched off by Pwren signal set low level and is switched on by Pwren signal set high.

Note: 1 For any other default output voltages, please contact your local ST-NXP Wireless sales.

Vsdc2 DC/DC converter supply voltage

Vsdc2 is a step-down converter with a very high efficiency.

1.8 V voltage level enables to supply all I/O voltages or any other voltage requested by the application.

Vsdc2 has 2 modes:

- high power mode (HPM) to supply the application,
- low power mode (LPM) to switch off the output voltage.

The power supply is switched off by Pwren signal set low and is switched on by Pwren signal set high.

2.9.2 LDO regulators

Vdig LDO regulator

Vdig LDO regulator has the same adjustment levels as Vsdc1.

Vdig is switched on at start-up and remains on when the application is power supplied.

Output voltage levels are adjustable via the Vsdc1 dedicated registers.

Vana1 LDO regulator

Vana1 is a LDO regulator with 1.8 V output voltage level.

Vana1 is switched on at start-up and remains always on when the application is power supplied.

Vana2, Vana4 LDO regulators

Vana2, Vana4 (Vana2/4) are adjustable LDO regulators with four output voltage levels used to supply different application peripherals.

Vana2/4 are turned on after Pon = 1 and Pwren =1, in that case the two power supplies are controlled by En_Vana(i) bit set high by default (*Note 1*) - *Power control register @ 07h*, En_Vana4 and *Power control register @ 08h* - En_Vana2.

If Vana2/4 need to be controlled directly by I2C, the converters are controlled by pdn_vana(i) bit in *Application controls register 1 @ 10h* - pdn_vana2 and *Application controls register 2 @ 11h* - and Pdn_Vana4.

The pdn_vana(i) bit and En_Vana(i) control bit are OR-gated features.

Vana2/4 high and low power modes are enabled by register *Power control register @ 09h* - Vana2_OFF, Vana4_OFF (*Note 1*).

Output voltage levels are adjustable by connecting the dedicated pins Vana2/4_Sel_0 and Vana2/4_Sel_1 to battery voltage or to the ground.

Vana3 LDO regulator

Vana3 is an adjustable LDO regulator with four output voltage levels used to supply different application peripherals. Vana3 is turned on after Pon = 1 and Pwren =1.

Vana3 has high power and low power modes enabled by register *Power control register @ 09h* vana3_OFF) (*Note 1*).

Output voltage levels are adjustable by connecting the dedicated pins Vana3_Sel_0 and vana3_Sel_1 to battery voltage or to the ground.

Table 6. Selection table

Vana(i)_Sel_1	Vana(i)_Sel_0	Output voltage (V)
0	0	1.8
0	1	2.5
1	0	2.8
1	1	3.3

Note: 1 For the different possible configurations of the Vana(i) supplies, please contact directly your ST-NXP Wireless sales office.

2.10 Thermal shutdown

A thermal sensor monitors the device temperature. This sensor is placed near the hottest part of the device. When the temperature exceeds the thermal threshold, the supplies are turned off. The supplies are turned back to their default start-up state, starting on Pon = 1, after around 10 ms (device at room temperature (25°C). The device mode changes back to normal and is ready to be controlled by I2C.

Table 7. Supplies thermal shutdown

Description	Min.	Typ.	Max.	Unit
Supply thermal threshold		150		°C

3 Electrical characteristics

Otherwise specified typical electrical characteristics have been defined for 25°C ambient temperature and 3.6 V battery voltage.

3.1 Absolute maximum rating

Table 8. Absolute maximum ratings

Parameter	Condition	Min.	Typ.	Max.	Unit
Input supply operating voltage		2.7	3.6	5.5	V
Input supply maximum rating voltage		2.7		7	V
VddIO rating voltage		1.65	1.8	1.84	V
Operating temperature		-30		+85	°C
Junction operating temperature	Spec. is guaranteed up to 125°C			+125	°C
Junction rating temperature				+150	°C
Consumption in off mode (Pon = 0)	Vbat = 3.6 V			10	µA
Consumption in sleep mode	At 25°C, Vbat = 3.6V Pon = 1 and Pwren = 0		180		µA
ESD	HBM JESD22-A114-B	-2		+2	kV
	CDM ANSI-ESDSM5.3.1-1999	-300		+500	V
Package Rth			70		°C/W

3.2 Electrical characteristics

3.2.1 Step-down converters

Table 9. Vsdc1 electrical characteristics

Parameter name	Condition	Min.	Typ.	Max.	Unit
Vsupply		2.7		5.5	V
Output voltage	16 steps	-5%	1.0 to 1.5	+5%	V
Vripple	Output voltage ripple		10		mVpp
Output load current		0		600	mA
Efficiency			86		%
Short circuit limitation(1)		0.9	1.2	1.4	A
Quiescent current(2)				5	µA
Power-down current				1.5	µA
Switching frequency			900		kHz
PSRR(1)	1kHz < f < 10kHz	40			dB
Rising slope	Iout = 10mA		0.3		ms/V
Line regulation	Vbat [2.7, 5.5V]			10	mV
Load regulation	Iout [0.1, 600mA]			10	mV
Line transient(1)	Vsdc1 = 1.2V Iout = 200mA ∆Vbat = 300mV Tr = tf = 10µs		7		mV
Load transient(1)	Vsdc1 = 1.2V Iout = [1, 400mA] Tr = tf = 100ns		70		mV

1. Guaranteed by design
2. Quiescent current defined as the current measured on the Vsdc1 dedicated power supply

Table 10. Vsdc2 electrical characteristics

Parameter name	Condition	Min.	Typ.	Max.	Unit
Vsupply		2.7		5.5	V
Output voltage		3%	1.8	+3%	V
Vripple	Output voltage ripple		10		mVpp
Output load current		0		600	mA
Efficiency			90		%
Short circuit limitation(1)		0.9	1.2	1.4	A
Quiescent current(2)				5	µA
Power-down current				1.5	µA
Switching frequency			900		kHz
PSRR(1)	1kHz < f < 10kHz	40			dB
Rising time (10 to 90%)			0.5		ms
Line regulation	Vbat [2.7, 5.5V]			10	mV
Load regulation	Iout [0.1, 600mA]			10	mV
Line transient(1)	Vsdc2 = 1.8V Iout = 200mA ΔVbat = 300mV Tr = tf = 10µs		7		mV
Load transient(1)	Vsdc2 = 1.8V Iout = [1, 400mA] Tr = tf = 100ns		70		mV

1. Guaranteed by design
2. Quiescent current defined as the current measured on the Vsdc2 dedicated power supply

3.2.2 Low-drop output converters

Table 11. Vana1 electrical characteristics

Parameter name	Condition	Min.	Typ.	Max.	Unit
Vsupply		2.7		5.5	V
Output voltage		-3%	1.8	+3%	V
Output load current				150	mA
Short circuit limitation(1)		230	340	550	mA
Quiescent current(2)	No load			30	µA
Power-down current				1	µA
Power supply rejection(1)	f < 20kHz f < 100kHz		50 45		dB
Rising time (10 to 90%)	Output voltage 1.8V Iout = 10mA		0.5		ms
Line regulation	Vbat [2.7, 5.5V]			5	mV
Load regulation	Iout [0.1, 150mA]			10	mV
Line transient(1)	Vana1= 1.8V Iout = 150mA ΔVbat = 300mV Tr = tf = 10µs		2		mV
Load transient(1)	Vsdc2 = 1.8V Iout = [1, 150mA] Tr = tf = 1µs		20		mV

1. Guaranteed by design
2. Quiescent current defined as the current measured on the Vana1 dedicated power supply

Table 12. Vana2/3/4 electrical characteristics

Parameter name	Condition	Min.	Typ.	Max.	Unit
Vsupply		Max[Vana(i)+0.2V, Vbat_min]		5.5	V
Output voltage		-3%	1.8 2.5 2.8 3.3	+3%	V
Output load current				150	mA
Short circuit limitation(1)		230	340	550	mA
Quiescent current(2)	No load			30	µA
Power-down current				1	µA
Power supply rejection(1)	f < 20kHz f < 100kHz	50 45			dB

Table 12. Vana2/3/4 electrical characteristics (continued)

Parameter name	Condition	Min.	Typ.	Max.	Unit
Rising slope for Vana4			20		µs/V
Rising slope	Iout = 10mA		0.3		ms/V
Line regulation	Vbat [2.7, 5.5V]			5	mV
Load regulation	Iout [0.1, 150mA]			10	mV
Line transient(1)	Vana1= 2.8V Iout = 150mA ΔVbat = 300mV Tr = tf = 10µs		2		mV
Load regulation(1)	Vsdc2 = 1.8V Iout = [1, 150mA] Tr = tf = 1µs		20		mV

1. Guaranteed by design
2. Quiescent current defined as the current measured on the Vana2/3 dedicated power supply

Table 13. Vdig electrical characteristics

Parameter name	Condition	Min.	Typ.	Max.	Unit
Vsupply		2.7		5.5	V
Output voltage		-3%	1.0 to 1.5	+3%	V
Output load current				250	mA
Short circuit limitation(1)		330	800		mA
Quiescent current(2)	No load			43	µA
Power-down current				1.5	µA
Rising slope	Iout = 10mA		0.3		ms/V
Line regulation	Vbat [2.7, 5.5V]			5	mV
Load regulation	Iout [0.1, 150mA]			10	mV
Line transient(1)	Vdig = 1.2V Iout = 150mA ΔVbat = 300mV Tr = tf = 10µs		1		mV
Load transient(1)	Vdig = 1.2V Iout = [1, 150mA] Tr = tf = 1µs		40		mV

1. Guaranteed by design
2. Quiescent current defined as the current measured on the Vdig dedicated power supply

3.2.3 DC/DC converter monitoring characteristics

Table 14. Vsdc1/2 monitoring output levels

Symbol	Description	Test conditions	Min.	Typ.	Max.	Units
Threshold						
T_{HCORE}	Threshold Vsdc1	Vsdc1 = 1.2V or 1.5V	-3%	Vsdc1-150	+3%	mV
		Vsdc1 = 1V	-3%	Vsdc1-100	+3%	mV
T_{HVIO}	Threshold Vsdc2		-3%	1.65	+3%	V

3.3 Digital specification

All electrical specifications using VddIO voltage as reference are able to sustain 1.8 V ± 5%.

3.3.1 CMOS input/output static characteristics: I2C interface

Table 15. CMOS input/output static characteristics: I2C interface

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
I2C interface						
Vil	Low level input voltage				0.3xVio	V
Vih	High level input voltage		0.7xVio			V
Iil	Low level input current		-1.0		+1.0	µA
Iih	High level input current		-1.0		+1.0	µA
Vol	Low level output voltage	Iol = 3mA (with open drain or open collector)			0.2xVio	V
Voh	High level output voltage	Iol = 3mA (with open drain or open collector)	0.8xVio			V

3.3.2 CMOS input/output dynamic characteristics: I2C interface

Table 16. CMOS input/output dynamic characteristics: I2C interface

Symbol	Description	Min.	Typ.	Max.	Unit
I2C interface					
Fscl	Clock frequency			400	kHz
Thigh	Clock pulse width high	600			ns
Tlow	Clock pulse width low	1300			ns
tr	SDA, SCL rise time	20+0.1Cb(1)		300	ns
tf	SDA, SCL rise time	20+0.1Cb(1)		300	ns
Thd_sta	Start condition hold time	600			ns
Tsu_sta	Start condition set up time	600			ns
Thd_dat	Data input hold time	0			ns
Tsu_dat	Data input set up time	100			ns
Tsu_sto	Stop condition set up time	600			ns
tbuf	Bus free time	1300			ns
Cb	Capacitive load for each bus line			400	pF

1. Cb = total capacitance of one bus line in pF

3.3.3 CMOS input/output static characteristics: VddIO level

Table 17. VddIO level: control I/Os

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
SW_reset, VddOK, Res_pro, Pwren						
Vil	Low level input voltage				0.3xVio	V
Vih	High level input voltage		0.7xVio			V
Iil	Low level input current		-1.0		1.5	µA
Iih	High level input current		-1.0		1.5	µA
Cin	Input capacitance				10	pF
Vol	Low level output voltage	Iol = 4mA			0.2xVio	V
Voh	High level output voltage	Iol = 4mA	0.8xVio			V
Tof	Output fall time				1	ns
Tor	Input fall time				1	ns
Ci/o	Driving capability				100	pF

3.3.4 CMOS input static characteristics: Vbat level

Table 18. CMOS input static characteristics: Vbat level

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
Vana2_sel[0:1], Vana3_sel[0:1], Vana4_sel[0:1], Vbat_Min_Thr_[0,1], Vbat_Max_Thr_[0,1], Vram_Sel, Vbat_Thr_Sel						
Vil	Low level input voltage				0.3xVbat	V
Vih	High level input voltage		0.7xVbat			V
Iil	Low level input current		-1.0		1.5	µA
Iih	High level input current		-1.0		1.5	µA
Cin	Input capacitance				10	pF

3.3.5 NMOS input Pon

Table 19. Pon input static characteristics

Symbol	Description	Test condition	Min.	Typ.	Max.	Unit
Pon						
Vil	Low level input voltage				0.5	V
Vih	High level input voltage		1		Vbat	V
Iil	Low level input current		-1.0		1.5	µA
Iih	High level input current		-1.0		1.5	µA

4 I2C interface

The I2C interface is used to control the power supplies and features of the battery charger.

The I2C bus is configured as a slave serial interface compatible with the I2C register trademark of Philips Inc (version 2.1).

The device is a slave serial interface with a data line (SDA) and a clock line (SCL):

- SCL is the input clock used to shift the data,
- SDA is the input/output bidirectional data transfer line.

The internal bus connection is composed of:

- one filter to reject spike on the bus data line and preserve data integrity,
- one bidirectional data transfer up to 400 kbit/s (fast mode) via SDA signal.

The SDA signal contains the input/output control and data signals that are shifted in the device MSB first. The first bit must be high (START) followed by the device ID (7 bits). A read/write bit control '1' indicates read access while a logical '0' indicates a write access.

Device ID:

- device ID in write mode: 5Ch
- device ID in read mode: 5Dh

The device sends an acknowledge at the end of an 8-bit transfer. The following 8-bit sequence corresponds to the register address followed by another acknowledge. The 8-bit data field is sent last and is also followed by a last acknowledge.

Table 20. Device ID

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AdrD6	AdrD5	AdrD4	AdrD3	AdrD2	AdrD1	AdrD0	R/W

Table 21. Register address

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RegADR7	RegADR6	RegADR5	RegADR4	RegADR3	RegADR2	RegADR1	RegADR0

Table 22. Register data

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

Figure 7. Control interface: I2C format

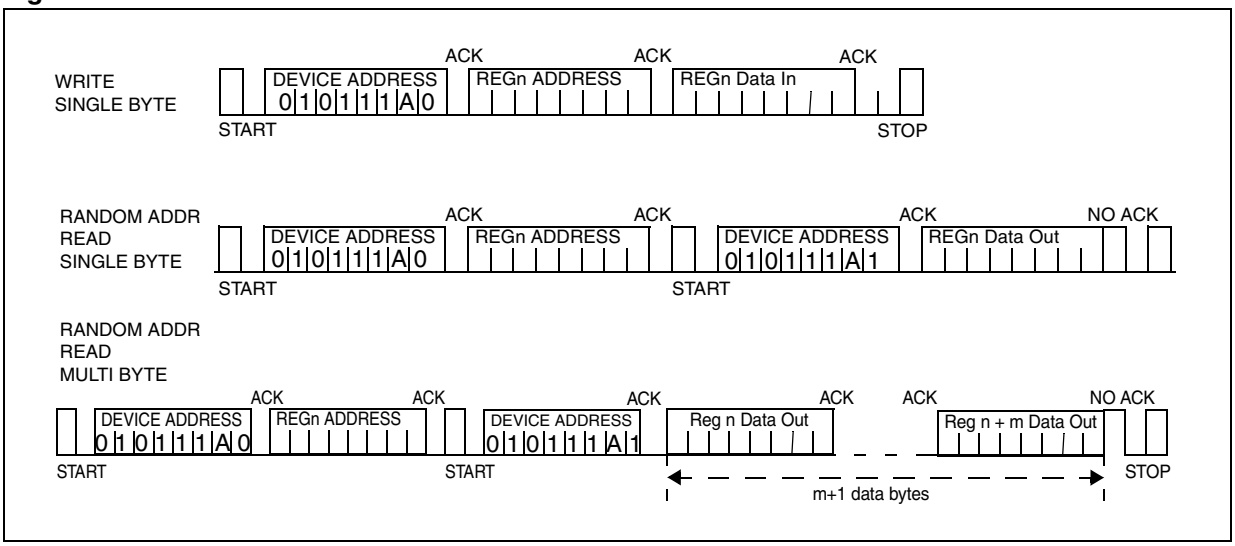
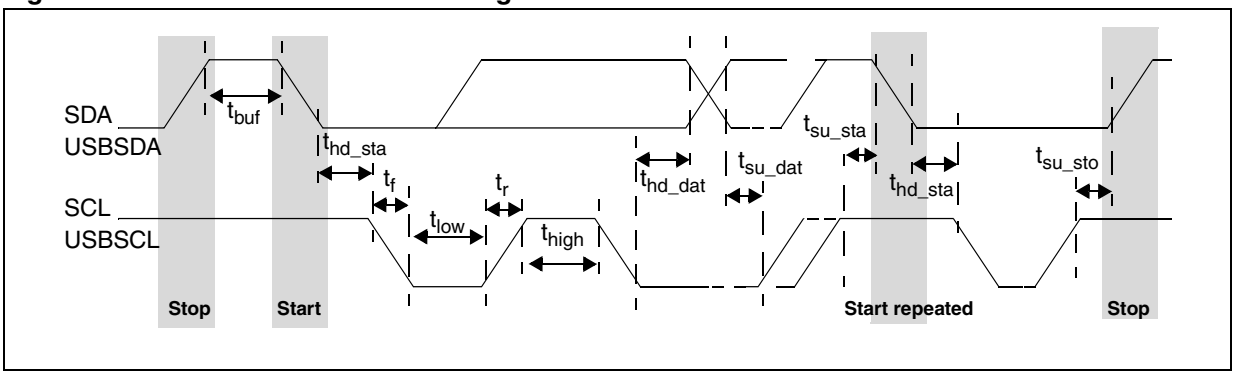


Figure 8. Control interface: I2C timing



Note: Multi-write possibility is not available. For each data it is mandatory to send the address first.

5 Clock management

5.1 Internal oscillator

The device functions with internal clock at around 1 MHz to switch the step-down converters. This oscillator is operational as soon as Pon = 1.

5.2 Internal 32 kHz clock

The device state machine functions with a 32 kHz clock generated internally by dividing the internal oscillator frequency.

6 Application hints

6.1 Application and external components

The application diagram shown in *Figure 9* illustrates an example where LDO is at 3.3 V and the battery supervisor threshold is respectively at 2.85 V and 3.5 V voltage values. Vram is supplied by Vsdc2 DC/DC converter at 1.8 V.

Figure 9. Application diagram example

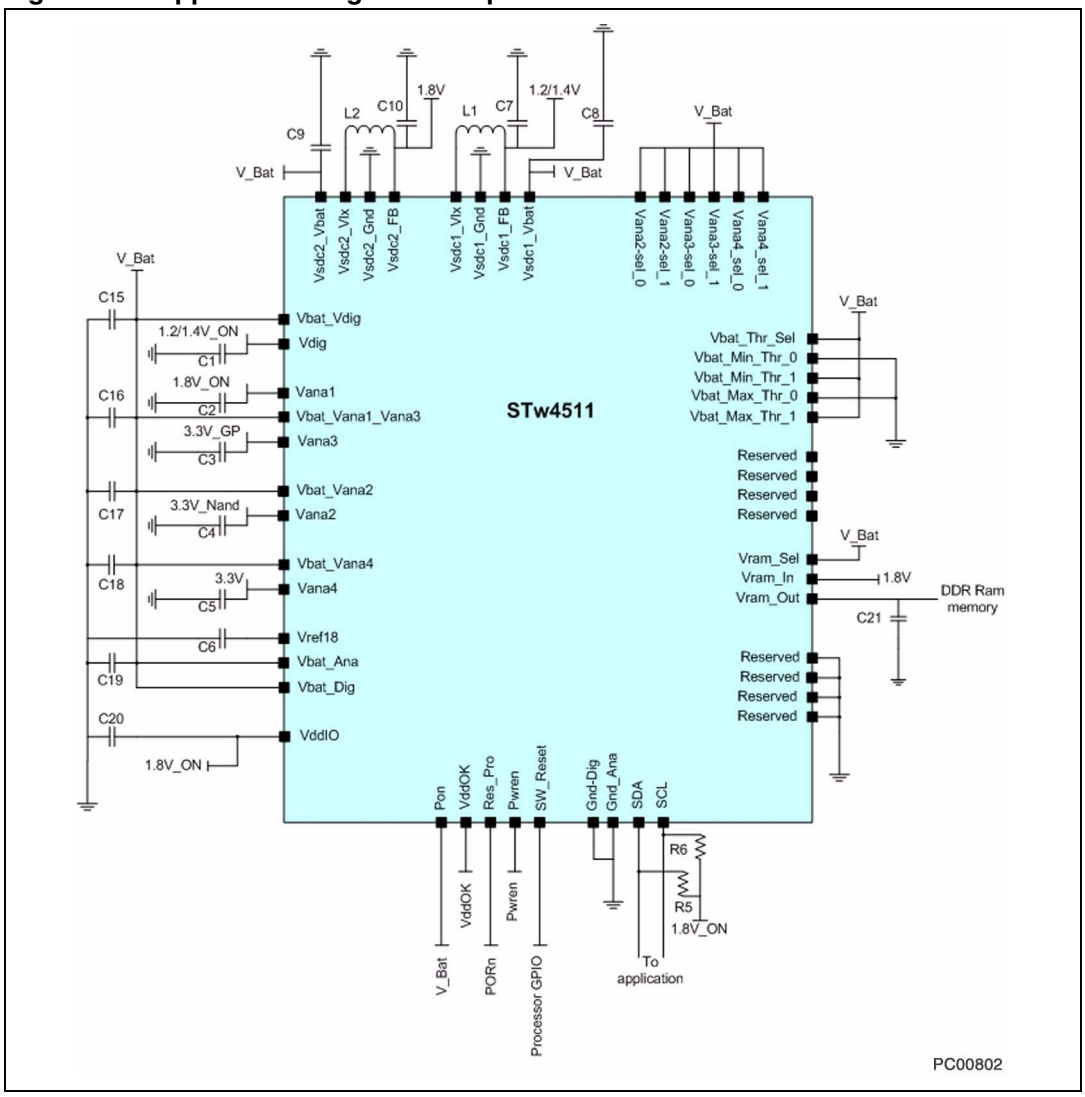


Table 23. List of materials

Name	Typ.	Units	Comments
L1 and L2	4.7	µH	Vsdc1 and Vsdc2 coils
C7 and C10	22	µF	Vsdc1 and Vsdc2 output capacitors, X5R type
C8 and C9	10	µF	Vsdc1 and Vsdc2 input capacitors, X5R type
C1, C2, C3, C4, C5	2.2	µF	LDO output capacitors
C15, C16, C17, C18	1	µF	LDO input capacitors
C6	2.2	µF	Vref capacitor
C19	10	µF	VddIO bypass capacitor
C20	1	µF	Analog supply bypass capacitor
C21	20	µF	DRAM memory maximum decoupling capacitor value
R5 and R6	2.2	kΩ	I2C pull-up resistors

Note: The production dispersion, temperature range, biasing and aging must be considered for all the above-listed components.

7 Register definition and mapping

The set of registers used to program the device are accessible via the 5Ch I2C address.

Table 24. Register general information

Address	Type	Comment
00h, 01h, 02h		Reserved
03h	R	Device version ID
10h	R/W	Application control register 1
11h	R/W	Application control register 2
12h to 1Dh		Test registers
1Eh to 1Fh	R/W	Power control registers

Table 25. Register summary

Register	Addr.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device version ID	03h	0	1	0	0	0	0	0	1
Application control register 1	10h	RESERVED						PDN_VANA2	RESERVED
Application register 2	11h	PDN_VANA1	RESERVED	MONITORING_VSDC1/2	0	RESERVED	RESERVED	RESERVED	PDN_VANA4

Register	15	14	13	12	10	9	8	7	6	5	4	3	2	1	0
Power control	RESERVED					REG_ADDRESS_2BIT		REG_ADDRESS_3BIT			DATA_IN/OUT_4BIT				EN
Address	1Fh							1Eh							

Note: Register 1Fh must be sent to the I2C before the register 1Eh (MSB address must be sent first).

Application controls register 1 @ 10h

7	6	5	4	3	2	1	0
RESERVED						PDN_VANA2	RESERVED

Address: 10h

Type: R/W

Reset: 0000_0000

Description:

[7:2] RESERVED

[1] PDN_VANA2
0: Vana2 in power off (default)1: Vana2 in HPM

[0] RESERVED

Application controls register 2 @ 11h

7	6	5	4	3	2	1	0
PDN_VANA1	RESERVED	MONITORING_VSDC1/2	RESERVED				PDN_VANA4
RW	R	R(1)	R				RW

1. Will be reset after reading

Address: 11h

Type: RW

Reset: 0000 0000

Description:

[7] PDN_VANA1
0: Vana1 in power down mode (default)1: Vana1 in high power mode

[6] RESERVED

[5] MONITORING_VSDC1/2
0: output in the good range (default)
1: output lower than expected on Vsdc1 or Vsdc2

[4:1] RESERVED

[0] PDN_VANA4
0: Vana4 in power down mode (default)
1: Vana4 in high power mode

Power control register @ 1Eh

7	6	5	4	3	2	1	0
REGISTER_ADDRESS_3BIT			DATA_IN_OUT_4BIT				EN

Address: 1Eh

Type: RW

Reset: 0000 0000

Description:

[7:5] REGISTER_ADDRESS_3BIT
See “Address” column (LSB) table (default =0)

[4:1] DATA_IN_OUT_4BIT
See control register table (default = 0)

[0] EN
0: Read enabled (default)1: write enabled

Power control register @ 1Fh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						REG_ADDRESS_2BIT		RESERVED							

Address: 1Fh

Type: RW

Reset: 0000 0000

Description:

[15:8] Reserved

[9:8] REG_ADDRESS_2BIT
See “Address” column (MSB) table (default = 0)

Power control register mapping

Table 26. Power control register mapping

Address 1Fh											Address 1Eh					Comment
RESERVED						REG_ADDRESS					DATA_IN/OUT				EN	
						2-bit MSB		3-bit LSB								
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
						00h to 04h										Test purpose
						05h to 09h					Setting					*Power control register @ 05h* to *Power control register @ 09h*
						0Bh to 1Eh										Test purpose

Power control register @ 05h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						0	0	1	0	1	VSDC1_VDIG[3:0]				EN

Address: 05h

Type: RW

Reset: 0000 0000 1011 1100

Description:

[15:10] Reserved

[4:1] VSDC1_VDIG_PRG[3:0]
0000 1.00V0001 1.05V
0010 1.10V0011 1.15V
0100 1.20V0101 1.22V
0110 1.24V0111 1.26V
1000 1.28V1001 1.30V
1010 1.32V1011 1.34V
1100 1.36V1101 1.38V
1110 1.40V (default)1111 1.50V

[0] EN
0 read enabled (default)1 write enabled

Power control register @ 06h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						0	0	1	1	0	1	EN_VDIG	1	1	EN
R											R	R	R	R	RW

Address: 06h

Type: RW

Reset: 0000 0000 1101 1110

Description:

[15:10] RESERVED

[4] 1 Default value = 1

[3] EN_VDIG
0: Vdig in power down mode
1: Vdig in high power mode (default)

[2] 1 Default value = 1

[1] 1 Default value = 1

[0] EN
0: Read enabled (default)1: Write enabled

Power control register @ 07h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						0	0	1	1	1	EN_VANA3	RESERVED	EN_VANA4	RESERVED	EN
R						R	R	R	R	R	RW	R	RW	R	RW

Address: 07h

Type: RW

Reset: 0000 0000 1111 0110

Description:

[15:10] RESERVED

[4] EN_VANA3
0: Vana3 in power down mode
1: Vana3 in high power mode (default)

[3] RESERVED

[2] EN_VANA4
0: Vana4 in power down mode
1: Vana4 in high power mode (default)

[1] RESERVED

[0] EN
0: Read enabled (default)1: Write enabled

Power control register @ 08h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						0	1	0	0	0	RESERVED	EN_MONITORING	EN_VANA2	RESERVED	EN
R						R	R	R	R	R	R	R	RW	R	RW

Address: 08h

Type: RW

Reset: 0000 0001 0000 1100

Description:

[15:10] RESERVED

[4] RESERVED

[3] EN_MONITORING
0: Disabled/monitoring = OFF
1: Enabled/Vsdc1 and Vsdc2 monitoring = 0N (default)

[2] EN_VANA2
0: Vana2 in power down mode
1: Vana2 enabled in high power mode (default)

[1] RESERVED

[0] EN
0: Read enabled (default)1: Write enabled

Power control register @ 09h

Address 1Fh								Address 1Eh							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						0	1	0	0	1	VANA2/3_OFF	0	RESERVED	VANA4_OFF	EN
R						R	R	R	R	R	RW	R	R	WR	RW

Address: 09h

Type: RW

Reset: 0000 0001 0011 1010

Description:

[15:10] RESERVED

[9] 0: default value = 0

[8] 1: default value = 1

[7] 0: default value = 0

[6] 0: default value = 0

[5] 1: default value = 1

[4] VANA2_VANA3_OFF: when Pwren = 0
0: VANA2 and VANA3 stay in HPM
1: VANA2 and VANA3 go in OFF mode (default)

[3] 0: default value = 0

[2] RESERVED

[1] VANA4_OFF: when Pwren = 0
0: VANA4 stay in HPM
1: VANA4 go in OFF mode (default)

[0] EN
0: Read enabled (default)1: Write enabled

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 27. TFBGA 6mm x 6mm x 1.2mm with 0.5 mm pitch and 0.3 mm ball

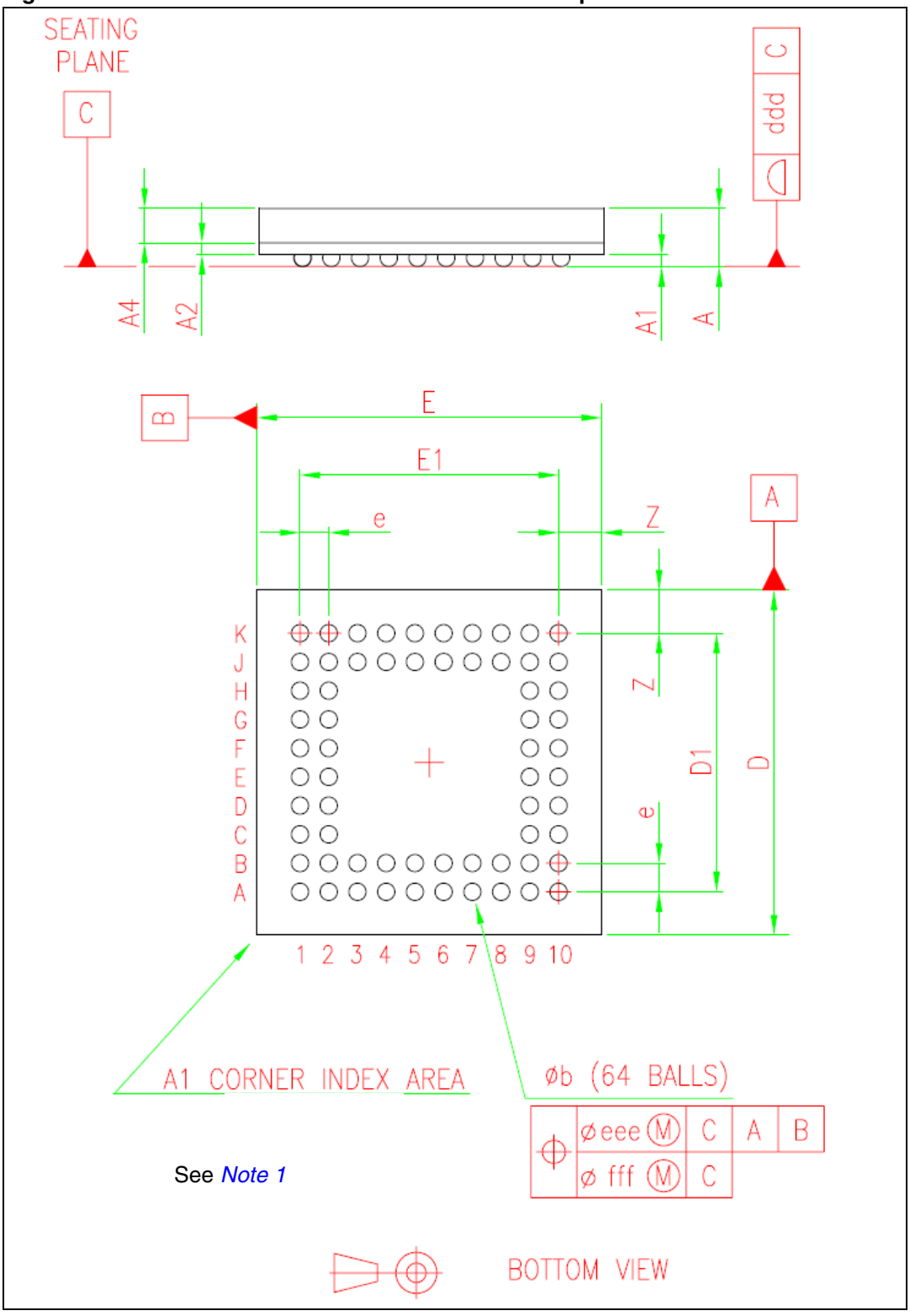
	Databook (mm)			Drawing (mm)		
Ref.	**Min.**	**Typ.**	**Max.**	**Min.**	**Typ.**	**Max.**
A(1)			1.20			1.06
A1	0.15			0.16	0.21	0.26
A2		0.20		0.16	0.20	0.24
A4		0.585		0.57	0.585	0.60
b(2)	0.25	0.30	0.35	0.25	0.30	0.35
D	5.85	6.00	6.15	5.90	6.00	6.10
D1		4.50			4.50	
E	5.85	6.00	6.15	5.90	6.00	6.10
E1		4.50			4.50	
e		0.50			0.50	
Z		0.75			0.75	
ddd			0.08			0.08
eee(3)			0.15			0.15
fff(4)			0.05			0.05

1. TFBGA stands for Thin profile Fine Pitch Ball Grid Array.
   Thin profile: $1.00mm < A \leq 1.20mm$/Fine pitch: $e < 1.00mm$ pitch.
   The total profile height (Dim A) is measured from the seating plane to the top of the component.
   The maximum total package height is calculated by the following methodology:

   $$A\ Max = A1\ Typ + A2\ Typ + A4\ Typ + \sqrt{(A1^2 + A2^2 + A3^2 tolerance\ values)}$$

2. The typical hall diameter before mounting is 0.30mm.
3. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each bail must lie within this tolerance zone.
4. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

Figure 10. TFBGA 6mm x 6mm x 1.2mm with 0.5 mm pitch and 0.3 mm ball



1. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

9 Ordering information

Table 28. Ordering information

Order code	Package	Packing
STW4511AH)/HF[1]	TFBGA 6mm x 6mm x 1.2mm	Tray
STW4511AH)T/HF	TFBGA 6mm x 6mm x 1.2mm	Tape and reel

1. ECOPACK® package

10 Revision history

Table 29. Document revision history

Date	Revision	Changes
26-Nov-2008	1	Initial release.

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