ISP1763A PCB design guidelines

AN3184

Application note

Abstract

This document describes the PCB design guidelines for the ISP1763A.

Keywords

isp1763a; host controller; peripheral controller; otg controller; usb; universal serial bus

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1 About this document

1.1 Purpose

This document provides the PCB design guidelines for the ISP1763A.

1.2 Revision information

Table 1 Revision history

Date	Rev.	Comments
2010-04-05	1	First version.
2010-08-18	2	Added Figure 7.
2013-07-18	3	Improved the quality of the PDF rendition, no other change in the content.
2013-10-02	4	Applied ST branding. No other change in the content.

1.3 Reference list

[1] *High Speed USB Platform Design Guidelines Rev. 1.0*

[2] *ISP1763A Hi-Speed USB OTG controller data sheet* *CD00264885*

[3] *Universal Serial Bus Specification Rev. 2.0* *www.usb.org*

2 Introduction

This document explains the design guidelines related to the ISP1763A USB OTG controller.

3 PCB layout recommendations

Some important checks for a successful PCB design are:

- Typically, a solution using four-layer PCB, signal 1, GND, V_{CC}, and signal 2, is sufficient for proper routing, allowing you to obtain good functionality and meeting all compliance tests requirements. Start your design by placing the ISP1763A, the major components, routing of the high-speed DP and DM traces, and clock traces. Also, a complete 'clean' solution to route the power and GND (plane split) must be defined before you start routing the rest of the signals.
- Route the high-speed USB differential pairs over continuous GND or power planes. Avoid crossing anti-etch areas and any breaks in internal planes (plane split). The minimum recommended distance to a plane split is 25 mils. Also, avoid placing a series of VIA holes near the DP and DM lines because these will create 'break areas' in the GND plane below. This is because of the clearance imposed by the manufacturing process around any VIA holes to an internal plane.
- Keep the length of the DP and DM traces equal. The maximum trace length mismatch between Hi-Speed USB signal pairs must not be greater than 70 mils.
- Maintain parallelism between USB differential signals, with the trace spacing needed to achieve 90-Ω differential impedance.
- Avoid corners when routing the differential pair DP and DM. Any 90° direction change of traces must be accomplished with two 45° turns or by using an arc of an imaginary circle tangent to the DP and DM lines.
- Avoid routing USB differential pairs near I/O connectors, signal headers, crystals, oscillators, magnetic devices, and power connectors.
- Maintain the maximum possible distance between high-speed USB differential pairs, high-speed or low-speed clock, and non-periodic signals. The minimum recommended distances are as follows:
  - 20 mils between the DP or DM trace, and low-speed non-periodic signal traces.
  - 50 mils between the DP or DM trace, and clock or high-speed periodic signal traces.
  - 20 mils between two pairs of the DP and DM traces.
- Route all the DP and DM lines on one layer. Do not change layers (avoid using VIAs) even to avoid crossing a plane split. It is better to place a non-split plane under high-speed USB signals, ground layer, or power layer. It is recommended that you place ground layer beneath the DP and DM lines.
- The maximum allowed length of the DP and DM lines for onboard solutions (or [trace + cable length] for a front-panel solution) is 18 inches.
- The decoupling capacitors must be placed as close as possible to the ISP1763A. A good choice is the four corners of the ISP1763A because these areas will not normally be occupied by traces or other components, according to the ISP1763A pinout.

- For good EMI testing results, it is recommended that you provide a good path from the USB connector shell to the chassis ground. The USB connector shell must be connected to an isolated ground plane.
- The common-mode choke used (if really necessary) on the DP and DM lines must be placed as close as possible to the USB connector and must have: Z_{com} < 8 Ω @ 100 MHz and Z_{diff} < 300 Ω @ 100 MHz. (Z_{diff} = 90 Ω ideally).
- Avoid using mechanical switch in series with DP or DM.

For more information, refer to *High Speed USB Platform Design Guidelines Rev. 1.0*.

4 Layout guideline for VFQFPN64 package

Figure 1 shows the bottom layer of the ISP1763A VFQFPN64 package. The encircled leads are the extended leads.

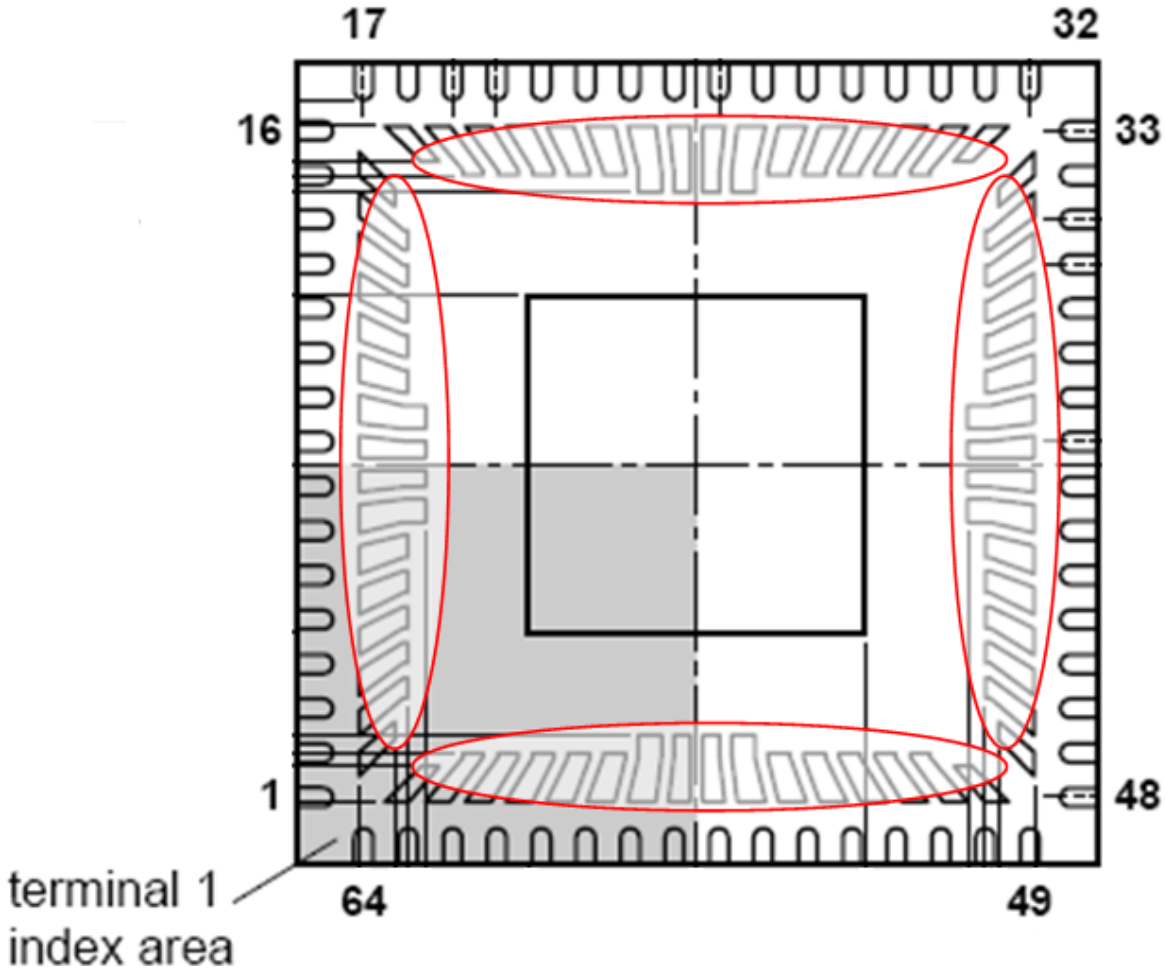

Figure 1 ISP1763A VFQFPN64 package bottom layer

At the bottom layer, there are 64 terminal leads that form the outer layer.

There is a centre GND pad that must be connected to the PCB electrical GND.

There are extended leads (encircled) between 64 terminal leads and the inner GND pad. These extended leads must not be connected to VIAs, traces, or any metal in the PCB routing. During assembling of the ISP1763A, take precautions to ensure that there are no solder between any of the extended leads.

4.1 Center GND pad

The center GND pad must be connected to the electrical GND of the PCB. See Figure 2.

It is better to have a through hole VIA on the PCB for the centre GND pad for manual assembly.

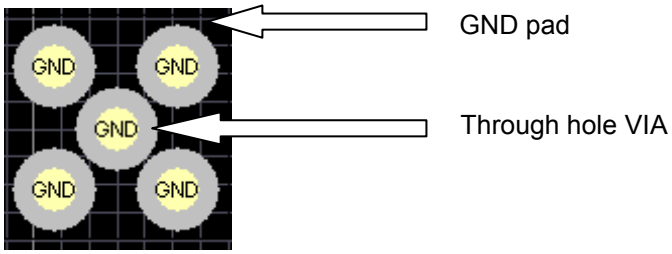

Figure 2 ISP1763A center GND pad

5 DP and DM routing recommendations

Note that the DP and DM trace length shown here is just a guideline. The trace length can vary depending on the printed circuit laminates and the thickness of traces. The trace length also largely depends on the components used on the DP and DM lines, such as ESD diodes and common mode choke coil. For example, if the ESD diode is used on the DP and DM lines, the trace length can be less than the guideline given in Section 5.2.

5.1 Routing DP and DM trace when USB connector is far from ISP1763A

Figure 3 shows additional guidelines for the DP and DM trace (straight) in the PCB layout when the distance between the USB connector and the ISP1763A is more than or equal to 3 inches.

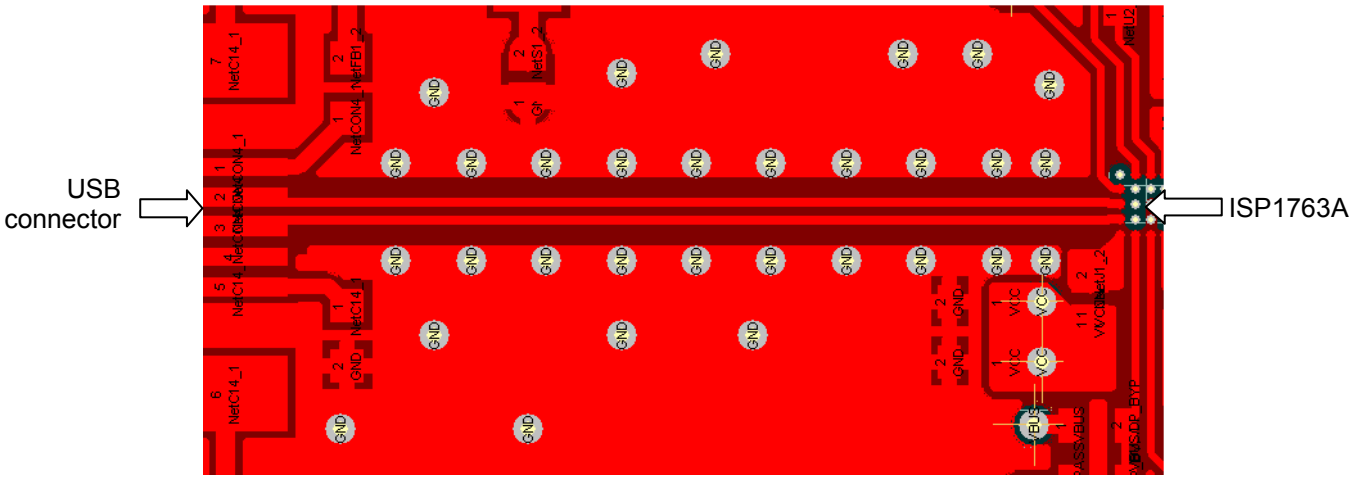

Figure 3 DP and DM layout

5.2 Routing DP and DM trace when USB connector is close to ISP1763A

Figure 4 shows additional guidelines for the DP and DM trace (zigzag) in the PCB layout when the distance between the USB connector and the ISP1763A is less than 3 inches. The zigzag trace is to accommodate the DP and DM lines of 3 inches within a smaller space.

The following example is based on the ISP1763A evaluation board.

- Copper 1 oz
- Trace width of DP and DM (W1) is 10 mils.
- Spacing between the DP and DM trace (S) is 6 mils.
- Distance between DP and DM to the ground plane (H) is 10 mils.

- Impedance control for DP and DM is 90 Ω.

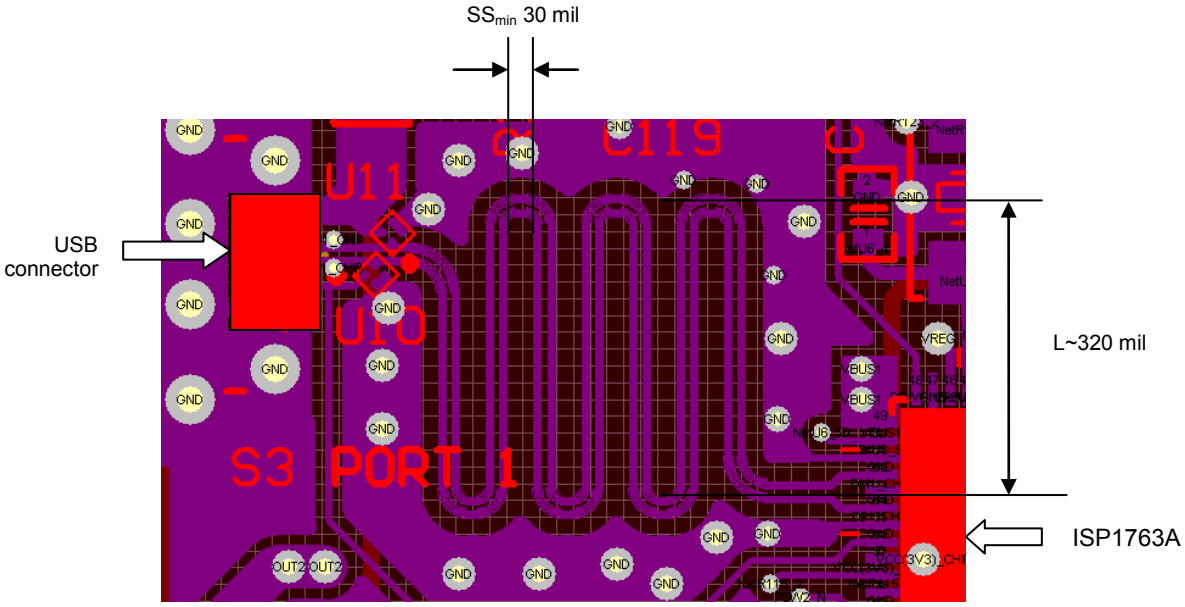

Figure 4 DP and DM layout with 3-inch length

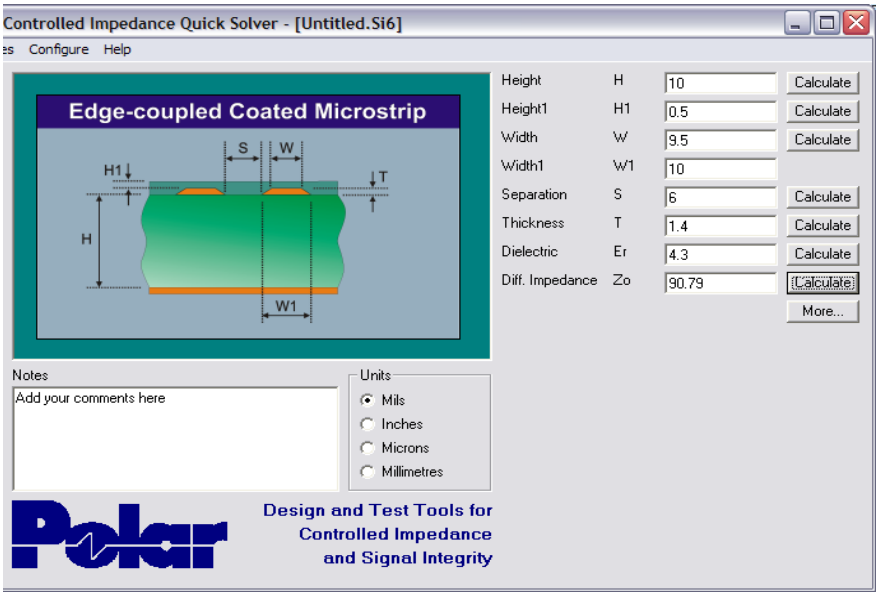

Figure 5 Impedance calculation

Table 2 PCB stack layer and dimension

PCB stack up			**Impedance (simulation result)**	
Layer	**Type**	**Thickness (mil)**		
Top side solder mask		**0.50 mils**	**Differential**	**Zo**
L1 (top)	Copper + plating	1.40 mils	DP trace = 10 mils Spacing = 6 mils DM trace = 10 mils	90.79 Ω
-	Prepreg	10.00 mils	-	-
L2	Copper	1.30 mils	-	-
-	Core	33.20 mils	-	-
L3	Copper	1.30 mils	-	-
-	Prepreg	10.00 mils	-	-
L4 (bottom)	Copper + plating	1.40 mils	-	-
Bottom side solder mask		**0.50 mils**		
Total		**59.60 mils**	**Material FR4**	
		1.51 mm		

5.3 ESD diode

The common-mode choke and ElectroStatic Discharge (ESD) protection components can be used if the design does not pass ElectroMagnetic Interference (EMI) or ESD tests because it may affect the signaling quality. Nevertheless, it is recommended to include necessary footprints for the common-mode choke and ESD protection components on the PCB as safeguards. Footprints must be placed as close as possible to the USB connector. Precautions must be taken when placing additional components on the DP and DM lines and routing recommendations must be followed.

The layout of ESD IC USBULC6-2F3 is shown in Figure 6.

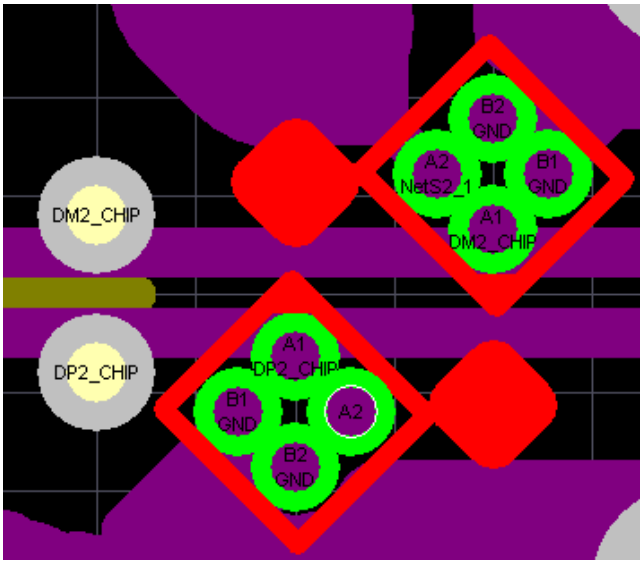

Figure 6 Layout of ESD IC USBULC6-2F3

6 ISP1763AHNUM footprint

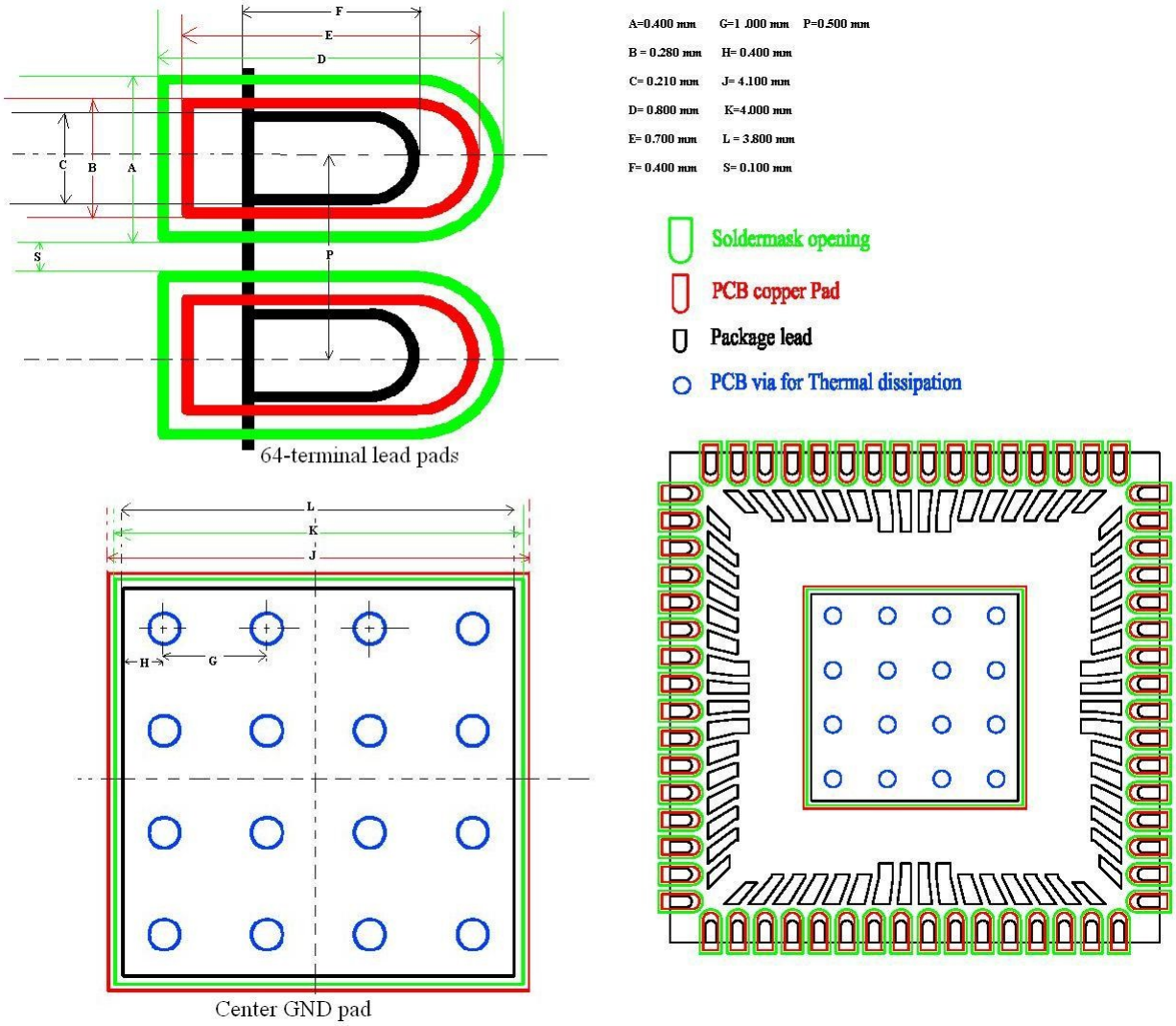

Figure 7 ISP1763AHNUM (VFQFPN6 package) footprint

Glossary

EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
PCB	Printed Circuit Board
USB	Universal Serial Bus