ISP1707A1 - USB TRANSCEIVER

ULPI Hi-Speed USB transceiver

The ISP1707A1 is a UTMI+ Low Pin Interface (ULPI) Hi-Speed Universal Serial Bus (USB) transceiver that is fully compliant with *Universal Serial Bus Specification Rev. 2.0*, *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*, *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*and *Battery Charging Specification Rev. 1.0*. It can transmit and receive USB data at high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps), and provides a pin-optimized, physical layer front-end attachment to the USB host, peripheral or OTG controller with Single Data Rate (SDR) ULPI link. The ISP1707A1 can transparently transmit and receive UART signaling. The ISP1707A1 is ideal for use in portable electronic devices, such as mobile phones, digital still cameras, digital video cameras, Personal Digital Assistants (PDAs) and digital audio players. It allows USB Application-Specific Integrated Circuits (ASICs), Programmable Logic Devices (PLDs) or any system chip set to interface with the physical layer of the USB through a 12-pin (SDR) interface. The ISP1707A1 can interface to devices with digital I/O voltages in the range of 1.65 V to 1.95 V.

KEY FEATURES

- Fully complies with:
  - USB: *Universal Serial Bus Specification Rev. 2.0*
  - OTG:*On-The-Go Supplement to the USB Specification Rev. 1.3*
  - ULPI:*UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
  - *Battery Charging Specification Rev. 1.0*
- Integrated battery charging detection circuit that operates during power-down mode to save current; the ISP1707A1 automatically detects if a USB battery charger is attached; this function can be disabled using external pins
- Interfaces to USB host, peripheral or OTG cores; optimized for portable devices or system ASICs with built-in ULPI link
- Complete Hi-Speed USB physical front-end solution that supports high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps)
  - Integrated 45 ohm ± 10 % high-speed termination resistors, 1.5 kohm ± 5 % full-speed device pull-up resistor, and 15 kohm ± 5 % host termination resistors
  - Integrated parallel-to-serial and serial-to-parallel converters to transmit and receive
  - USB clock and data recovery to receive USB data up to ±500 ppm
  - USB data synchronization from 60 MHz input to 480 MHz output during transmit
  - Insertion of stuff bits during transmit and discarding of stuff bits during receive
    Non-Return-to-Zero Inverted (NRZI) encoding and decoding
  - Supports bus reset, suspend, resume and high-speed detection handshake (chirp)
- Complete USB OTG physical front-end that supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)
  - Supports external charge pump or external V_{BUS}power switch
  - Complete control over USB termination resistors
  - Data line and V_{BUS} pulsing session request methods
  - Integrated V_{BUS} voltage comparators
  - Integrated cable (ID) detector
- Flexible system integration and very low power consumption, optimized for portable devices
  - 3.0 V to 4.5 V power supply input range; charger detection operates from V_{CC}2.55 V to 4.5 V
  - Internal voltage regulator supplies 2.7 V or 3.3 V and 1.8 V
  - Supports interfacing I/O voltage of 1.65 V to 1.95 V; separate I/O voltage supply pins minimize crosstalk
  - Both active-HIGH and active-LOW chip select pins are available
  - Power-down internal regulators in power-down mode when $V_{CC(I/O)}$ is not present or chip select is deasserted
  - Typical operating current of 13 mA to 34 mA, depending on the USB speed and bus utilization
  - Typical suspend current of 120 µA for 19.2 MHz and 145 µA for 26 MHz
  - Typical power-down state current of 5.5 µA
  - 3-state ULPI interface by the chip select, allowing bus reuse by other applications
- Highly optimized ULPI compliant
  - 60 MHz, 12-pin interface between the core and the transceiver, including an 8-bit SDR bus
  - Supports 60 MHz output clock configuration
  - Integrated Phase-Locked Loop (PLL) supporting crystal or clock frequencies of 19.2 MHz and 26 MHz
  - Crystal or clock frequency selectable by pin
  - Fully programmable ULPI-compliant register set
  - 3-pin or 6-pin full-speed or low-speed serial mode
  - Internal power-on reset (PoR) circuit
- UART interface:
  - Supports transparent UART signaling on pins DP and DM for the UART accessory application
  - 2.7 V UART signaling on pins DP and DM
  - Entering UART mode by register setting
  - Exiting UART mode by asserting pin STP or by toggling chip select
- Full industrial grade operating temperature range from -40 °C to +85 °C
- ESD compliance:
  - JESD22-A114D ±2 kV contact Human Body Model (HBM)
  - JESD22-A115-A ±200 V Machine Model (MM)
  - JESD22-C101-A ±500 V Charge Device Model (CDM)
  - IEC 61000-4-2, ±8.8 kV contact on pins DP and DM
  - IEC 61000-4-2 with IP4359CX4/LF, ±20 kV contact on the DP and DM pins
- Available in small TFBGA36 (3.5 mm × 3.5 mm) Restriction of Hazardous Substances (RoHS) compliant, halogen-free and lead-free package

APPLICATIONS

- Mobile phone
- Digital still camera
- MP3 player
- PDA
- Digital TV
- Digital versatile disc (DVD) recorder
- External storage device
- Printer
- Scanner
- Set-top box (STB)
- Video camera

CONTACT

For USB technical support and errata sheets (if any), contact wired.support@stericsson.com